SBOS263E − AUGUST 2004 − REVISED AUGUST 2007

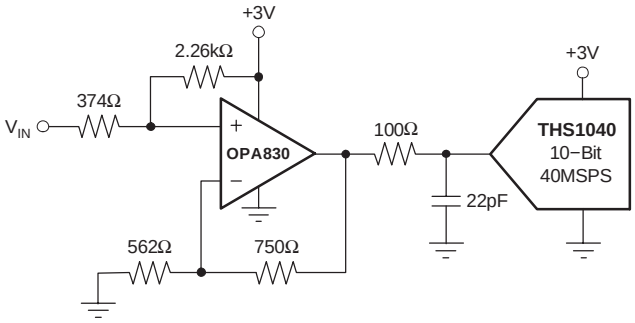
Low-Power, Single-Supply, Wideband Operational Amplifier

FEATURES

- **HIGH BANDWIDTH:**
  250MHz (G = +1)
  110MHz (G = +2)
- **LOW SUPPLY CURRENT: 3.9mA (V_S = +5V)**
- **FLEXIBLE SUPPLY RANGE:**
  ±1.4V to ±5.5V Dual Supply
  +2.8V to +11V Single Supply
- **INPUT RANGE INCLUDES GROUND ON SINGLE SUPPLY**
- **4.88V OUTPUT SWING ON +5V SUPPLY**
- **HIGH SLEW RATE: 550V/µs**
- **LOW INPUT VOLTAGE NOISE: 9.2nV/√Hz**
- **Pb-FREE SOT23 PACKAGE**

APPLICATIONS

- **SINGLE-SUPPLY ANALOG-TO-DIGITAL CONVERTER (ADC) INPUT BUFFERS**
- **SINGLE-SUPPLY VIDEO LINE DRIVERS**
- **CCD IMAGING CHANNELS**
- **LOW-POWER ULTRASOUND**
- **PLL INTEGRATORS**
- **PORTABLE CONSUMER ELECTRONICS**



DC-Coupled, +3V ADC Driver

DESCRIPTION

The OPA830 is a low-power, single-supply, wideband, voltage-feedback amplifier designed to operate on a single +3V or +5V supply. Operation on ±5V or +10V supplies is also supported. The input range extends below the negative supply and to within 1.7V of the positive supply. Using complementary common-emitter outputs provides an output swing to within 25mV of either supply while driving 150Ω. High output drive current (±80mA) and low differential gain and phase errors also make them ideal for single-supply consumer video products.

Low distortion operation is ensured by the high gain bandwidth product (110MHz) and slew rate (550V/µs), making the OPA830 an ideal input buffer stage to 3V and 5V CMOS ADCs. Unlike other low-power, single-supply amplifiers, distortion performance improves as the signal swing is decreased. A low 9.2nV/√Hz input voltage noise supports wide dynamic range operation.

The OPA830 is available in an industry-standard SO-8 package. The OPA830 is also available in an ultra-small SOT23-5 package. For fixed-gain line driver applications, consider the OPA832.

RELATED PRODUCTS

DESCRIPTION	SINGLES	DUALS	TRIPLES	QUADS
Rail-to-Rail	—	OPA2830	—	OPA4830
Rail-to-Rail Fixed Gain	OPA832	OPA2832	OPA3832	—
General-Purpose (1800V/µs slew rate)	OPA690	OPA2690	OPA3690	—
Low-Noise, High DC Precision	OPA820	OPA2822	—	OPA4820

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ABSOLUTE MAXIMUM RATINGS(1)

Power Supply	$12V_{DC}$
Internal Power Dissipation	See Thermal Analysis
Differential Input Voltage	±2.5V
Input Voltage Range (Single Supply)	−0.5V to $+V_S$ + 0.3V
Storage Temperature Range: D, DBV	−40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature (T_J)	+150°C
ESD Rating:	
Human Body Model (HBM)	2000V
Charge Device Model (CDM)	1500V
Machine Model (MM)	200V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

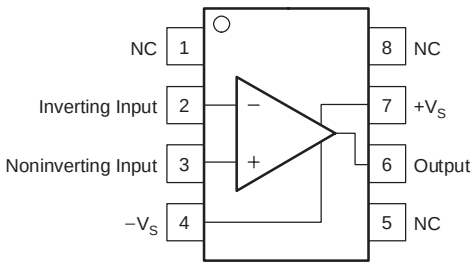
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA830	SO-8 Surface-Mount	D	−40°C to +85°C	OPA830	OPA830ID	Rails, 100
″	″	″	″	″	OPA830IDR	Tape and Reel, 2500
OPA830	SOT23-5	DBV	−40°C to +85°C	A72	OPA830IDBVT	Tape and Reel, 250
″	″	″	″	″	OPA830IDBVR	Tape and Reel, 3000

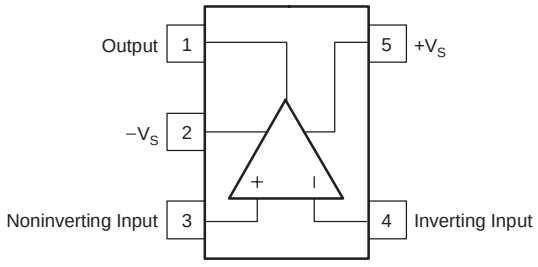
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

PIN CONFIGURATIONS

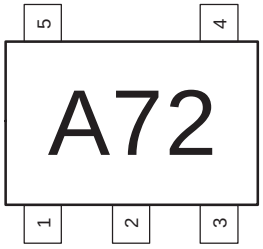


SO−8

NC = No Connection



SOT23−5



Pin Orientation/Package Marking

ELECTRICAL CHARACTERISTICS: $V_S = \pm5V$

Boldface limits are tested at **+25°C.**

At T_A = 25°C, G = +2, R_F = 750Ω, and R_L = 150Ω to GND, unless otherwise noted (see Figure 3).

PARAMETER	CONDITIONS	OPA830ID, IDBV				UNITS	MIN/ MAX	TEST LEVEL (3)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to 70°C(2)	−40°C to +85°C(2)			
AC PERFORMANCE (see Figure 3)								
Small-Signal Bandwidth	G = +1, $V_O \le 0.2V_{PP}$	310				MHz	typ	C
	G = +2, $V_O \le 0.2V_{PP}$	120	70	68	65	MHz	min	B
	G = +5, $V_O \le 0.2V_{PP}$	25	18	16	15	MHz	min	B
	G = +10, $V_O \le 0.2V_{PP}$	11	8	7	6	MHz	min	B
Gain-Bandwidth Product	G ≥ +10	110	85	82	80	MHz	min	B
Peaking at a Gain of +1	$V_O \le 0.2V_{PP}$	6				dB	typ	C
Slew Rate	G = +2, 2V Step	600	280	270	260	V/µs	min	B
Rise Time	0.5V Step	3.3	5.8	5.85	5.9	ns	max	B
Fall Time	0.5V Step	3.5	5.9	5.95	6.0	ns	max	B
Settling Time to 0.1%	G = +2, 1V Step	42	63	65	66	ns	max	B
Harmonic Distortion	$V_O = 2V_{PP}$, f = 5MHz							
2nd-Harmonic	R_L = 150Ω	−67	−59	−57	−56	dBc	max	B
	R_L ≥ 500Ω	−71	−62	−61	−60	dBc	max	B
3rd-Harmonic	R_L = 150Ω	−60	−50	−49	−48	dBc	max	B
	R_L ≥ 500Ω	−77	−65	−62	−59	dBc	max	B
Input Voltage Noise	f > 1MHz	9.5	10.5	11.0	11.5	nV/√Hz	max	B
Input Current Noise	f > 1MHz	3.7	4.7	5.2	5.7	pA/√Hz	max	B
NTSC Differential Gain		0.07				%	typ	C
NTSC Differential Phase		0.17				°	typ	C
DC PERFORMANCE(4)	R_L = 150Ω							
Open-Loop Voltage Gain		74	**66**	65	64	dB	min	A
Input Offset Voltage		±1.5	**±7**	±8.1	±8.6	mV	max	A
Average Offset Voltage Drift		—		±25	±25	µV/°C	max	B
Input Bias Current	V_{CM} = 0V	+5	**+10**	+12	+13	µA	max	A
Input Bias Current Drift				±12	±12	nA/°C	max	B
Input Offset Current	V_{CM} = 0V	±0.1	**±1**	±1.2	±1.4	µA	max	A
Input Offset Current Drift		—		±5	±5	nA/°C	max	B
INPUT								
Negative Input Voltage(5)		−5.5	**−5.4**	−5.3	−5.2	V	max	A
Positive Input Voltage(5)		3.2	**3.1**	3.0	2.9	V	min	A
Common-Mode Rejection Ratio (CMRR)	Input-Referred	80	**76**	74	72	dB	min	A
Input Impedance								
Differential Mode		10 ‖2.1				kΩ ‖pF	typ	C
Common-Mode		400 ‖1.2				kΩ ‖pF	typ	C
OUTPUT								
Output Voltage Swing	G = +2, R_L = 1kΩ to GND	±4.88	**±4.86**	±4.85	±4.84	V	min	A
	G = +2, R_L = 150Ω to GND	±4.64	**±4.60**	±4.58	±4.56	V	min	A
Current Output, Sinking and Sourcing		±85	**±65**	±60	±55	mA	min	A
Short-Circuit Current	Output Shorted to Ground	150				mA	typ	C
Closed-Loop Output Impedance	G = +2, f ≤ 100kHz	0.06				Ω	typ	C
POWER SUPPLY								
Minimum Operating Voltage		±1.4				V	typ	C
Maximum Operating Voltage			**±5.5**	±5.5	±5.5	V	max	A
Maximum Quiescent Current	$V_S = \pm5V$	4.25	**4.7**	5.3	5.9	mA	max	A
Minimum Quiescent Current	$V_S = \pm5V$	4.25	**4.0**	3.6	3.3	mA	min	A
Power-Supply Rejection Ratio (+PSRR)	Input-Referred	66	**61**	60	59	dB	min	A
THERMAL CHARACTERISTICS								
Specification: ID, IDBV		−40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}								
D SO-8		125				°C/W	typ	C
DBV SOT23-5		150				°C/W	typ	C

(1) Junction temperature = ambient for +25°C specifications.
(2) Junction temperature = ambient at low temperature limits; junction temperature = ambient +5°C at high temperature limit for over temperature specifications.
(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Current is considered positive out of pin.
(5) Tested < 3dB below minimum specified CMRR at ± CMIR limits.

ELECTRICAL CHARACTERISTICS: V_S = +5V

Boldface limits are tested at **+25°C.**

At T_A = 25°C, G = +2, R_F = 750Ω, and R_L = 150Ω to V_S/2, unless otherwise noted (see Figure 1).

PARAMETER	CONDITIONS	OPA830ID, IDBV				UNITS	MIN/ MAX	TEST LEVEL (3)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to 70°C(2)	−40°C to +85°C(2)			
AC PERFORMANCE (see Figure 1)								
Small-Signal Bandwidth	G = +1, $V_O \le 0.2V_{PP}$	250				MHz	typ	C
	G = +2, $V_O \le 0.2V_{PP}$	110	72	70	68	MHz	min	B
	G = +5, $V_O \le 0.2V_{PP}$	24	17	16	15	MHz	min	B
	G = +10, $V_O \le 0.2V_{PP}$	11	8	7	6	MHz	min	B
Gain-Bandwidth Product	G ≥ +10	110	84	80	79	MHz	min	B
Peaking at a Gain of +1	$V_O \le 0.2V_{PP}$	5				dB	typ	C
Slew Rate	G = +2, 2V Step	550	280	270	260	V/µs	min	B
Rise Time	0.5V Step	3.3	5.7	5.8	5.9	ns	max	B
Fall Time	0.5V Step	3.3	5.7	5.8	5.9	ns	max	B
Settling Time to 0.1%	G = +2, 1V Step	43	64	66	67	ns	max	B
Harmonic Distortion	$V_O = 2V_{PP}$, f = 5MHz							
2nd-Harmonic	R_L = 150Ω	−62	−55	−54	−53	dBc	max	B
	R_L ≥ 500Ω	−64	−58	−57	−56	dBc	max	B
3rd-Harmonic	R_L = 150Ω	−58	−50	−49	−48	dBc	max	B
	R_L ≥ 500Ω	−84	−66	−63	−60	dBc	max	B
Input Voltage Noise	f > 1MHz	9.2	10.2	10.7	11.2	nV/√Hz	max	B
Input Current Noise	f > 1MHz	3.5	4.5	5.0	5.5	pA/√Hz	max	B
NTSC Differential Gain		0.08				%	typ	C
NTSC Differential Phase		0.09				°	typ	C
DC PERFORMANCE(4)	R_L = 150Ω							
Open-Loop Voltage Gain		72	**66**	65	64	dB	min	A
Input Offset Voltage		±0.5	**±5.0**	±6.0	±6.5	mV	max	A
Average Offset Voltage Drift		—		±20	±20	µV/°C	max	B
Input Bias Current	V_{CM} = 2.5V	+5	**+10**	+12	+13	µA	max	A
Input Bias Current Drift				±12	±12	nA/°C	max	B
Input Offset Current	V_{CM} = 2.5V	±0.1	**±0.8**	±1	±1.2	µA	max	A
Input Offset Current Drift		—		±5	±5	nA/°C	max	B
INPUT								
Least Positive Input Voltage(5)		−0.5	**−0.4**	−0.3	−0.2	V	max	A
Most Positive Input Voltage(5)		3.2	**3.1**	3.0	2.9	V	min	A
Common-Mode Rejection Ratio (CMRR)	Input-Referred	80	**76**	74	72	dB	min	A
Input Impedance								
Differential-Mode		10 ‖2.1				kΩ ‖pF	typ	C
Common-Mode		400 ‖1.2				kΩ ‖pF	typ	C
OUTPUT								
Least Positive Output Voltage	G = +5, R_L = 1kΩ to 2.5V	0.09	**0.11**	0.12	0.13	V	max	A
	G = +5, R_L = 150Ω to 2.5V	0.21	**0.24**	0.25	0.26	V	max	A
Most Positive Output Voltage	G = +5, R_L = 1kΩ to 2.5V	4.91	**4.89**	4.88	4.87	V	min	A
	G = +5, R_L = 150Ω to 2.5V	4.78	**4.75**	4.73	4.72	V	min	A
Current Output, Sourcing and Sinking		±80	**±60**	±55	±52	mA	min	A
Short-Circuit Output Current	Output Shorted to Either Supply	140				mA	typ	C
Closed-Loop Output Impedance	G = +2, f ≤ 100kHz	0.06				Ω	typ	C
POWER SUPPLY								
Minimum Operating Voltage		+2.8				V	typ	C
Maximum Operating Voltage			**+11**	+11	+11	V	max	A
Maximum Quiescent Current	V_S = +5V	3.9	**4.1**	4.8	5.5	mA	max	A
Minimum Quiescent Current	V_S = +5V	3.9	**3.7**	3.4	3.1	mA	min	A
Power-Supply Rejection Ratio (PSRR)	Input-Referred	66	**61**	60	59	dB	min	A
THERMAL CHARACTERISTICS								
Specification: ID, IDBV		−40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}								
D SO-8		125				°C/W	typ	C
DBV SOT23-5		150				°C/W	typ	C

(1) Junction temperature = ambient for +25°C specifications.

(2) Junction temperature = ambient at low temperature limits; junction temperature = ambient +5°C at high temperature limit for over temperature.

(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

(4) Current considered positive out of pin.

(5) Tested < 3dB below minimum specified CMRR at ± CMIR limits.

ELECTRICAL CHARACTERISTICS: V_S = +3V

Boldface limits are tested at **+25°C.**

At T_A = 25°C, G = +2, and R_L = 150Ω to V_S/3, unless otherwise noted (see Figure 2).

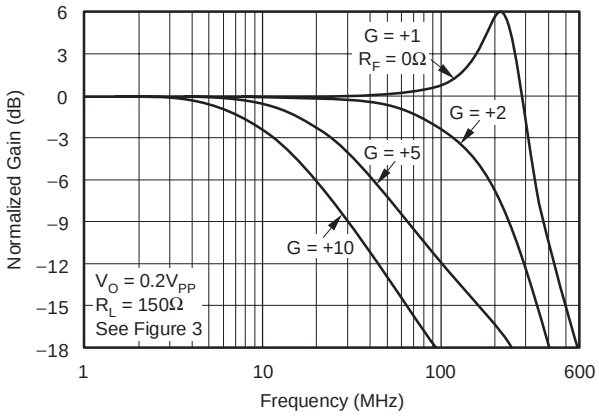
PARAMETER	CONDITIONS	OPA830ID, IDBV			UNITS	MIN/ MAX	TEST LEVEL (3)
		TYP	MIN/MAX OVER TEMPERATURE				
		+25°C	+25°C(1)	0°C to 70°C(2)			
AC PERFORMANCE (see Figure 2)							
Small-Signal Bandwidth	G = +2, $V_O \le 0.2V_{PP}$	100	72	68	MHz	min	B
	G = +5, $V_O \le 0.2V_{PP}$	22	17	16	MHz	min	B
	G = +10, $V_O \le 0.2V_{PP}$	10	8	7	MHz	min	B
Gain-Bandwidth Product	G ≥ +10	100	80	76	MHz	min	B
Slew Rate	1V Step	225	140	110	V/µs	min	B
Rise Time	0.5V Step	3.3	5.5	5.6	ns	max	B
Fall Time	0.5V Step	3.3	5.5	5.6	ns	max	B
Settling Time to 0.1%	1V Step	45	72	87	ns	max	B
Harmonic Distortion	V_O = 1V_{PP}, f = 5MHz						
2nd-Harmonic	R_L = 150Ω	−67	−61	−59	dBc	max	B
	R_L ≥ 500Ω	−67	−61	−59	dBc	max	B
3rd-Harmonic	R_L = 150Ω	−66	−59	−58	dBc	max	B
	R_L ≥ 500Ω	−77	−59	−58	dBc	max	B
Input Voltage Noise	f > 1MHz	9.2	10.2	10.7	nV/√Hz	max	B
Input Current Noise	f > 1MHz	3.5	4.5	5.0	pA/√Hz	max	B
DC PERFORMANCE(4)							
Open-Loop Voltage Gain		72	**66**	65	dB	min	A
Input Offset Voltage		±1.5	**±7**	±8.1	mV	max	A
Average Offset Voltage Drift		—		±25	µV/°C	max	B
Input Bias Current	V_{CM} = 1.0V	+5	**+10**	+12	µA	max	A
Input Bias Current Drift				±12	nA/°C	max	B
Input Offset Current	V_{CM} = 1.0V	±0.1	**±1**	±1.2	µA	max	A
Input Offset Current Drift		—		±5	nA/°C	max	B
INPUT							
Least Positive Input Voltage(5)		−0.45	**−0.4**	−0.27	V	max	A
Most Positive Input Voltage(5)		1.2	**1.1**	1.0	V	min	A
Common-Mode Rejection Ratio (CMRR)	Input-Referred	80	**75**	73	dB	min	A
Input Impedance							
Differential-Mode		10 ||2.1			kΩ ||pF	typ	C
Common-Mode		400 ||1.2			kΩ ||pF	typ	C
OUTPUT							
Least Positive Output Voltage	G = +5, R_L = 1kΩ to 1.5V	0.08	**0.11**	0.125	V	max	A
	G = +5, R_L = 150Ω to 1.5V	0.17	**0.39**	0.40	V	max	A
Most Positive Output Voltage	G = +5, R_L = 1kΩ to 1.5V	2.91	**2.88**	2.85	V	min	A
	G = +5, R_L = 150Ω to 1.5V	2.82	**2.74**	2.70	V	min	A
Current Output, Sourcing		30	**20**	18	mA	min	A
Current Output, Sinking		30	**20**	18	mA	min	A
Short-Circuit Output Current	Output Shorted to Either Supply	45			mA	typ	C
Closed-Loop Output Impedance	See Figure 2, f < 100kHz	0.06			Ω	typ	C
POWER SUPPLY							
Minimum Operating Voltage		+2.8			V	min	B
Maximum Operating Voltage			**+11**	+11	V	max	A
Maximum Quiescent Current	V_S = +3V	3.7	**4.0**	4.7	mA	max	A
Minimum Quiescent Current	V_S = +3V	3.7	**3.3**	3.1	mA	min	A
Power-Supply Rejection Ratio (PSRR)	Input-Referred	64	**60**	58	dB	min	A
THERMAL CHARACTERISTICS							
Specification: ID, IDBV		−40 to +85			°C	typ	C
Thermal Resistance, θ_{JA}							
D SO-8		125			°C/W	typ	C
DBV SOT23-5		150			°C/W	typ	C

(1) Junction temperature = ambient for +25°C specifications.
(2) Junction temperature = ambient at low temperature limits; junction temperature = ambient +5°C at high temperature limit for over temperature.
(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Current considered positive out of pin.
(5) Tested < 3dB below minimum specified CMRR at ± CMIR limits.

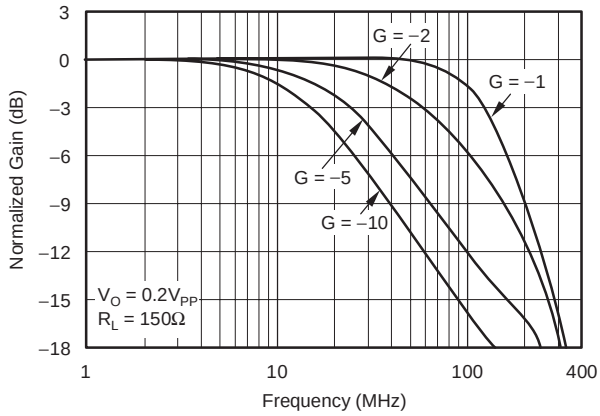
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$

At T_A = 25°C, G = +2, R_F = 750Ω, and R_L = 150Ω to GND, unless otherwise noted (see Figure 3).

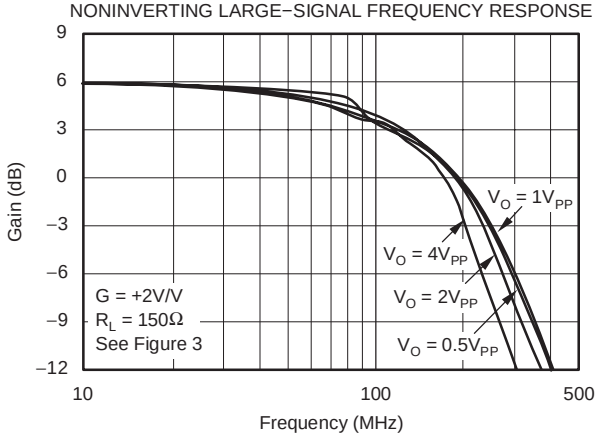
NONINVERTING SMALL−SIGNAL FREQUENCY RESPONSE



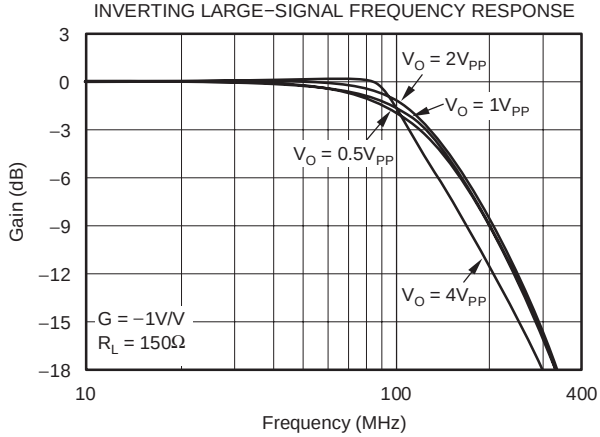
INVERTING SMALL−SIGNAL FREQUENCY RESPONSE



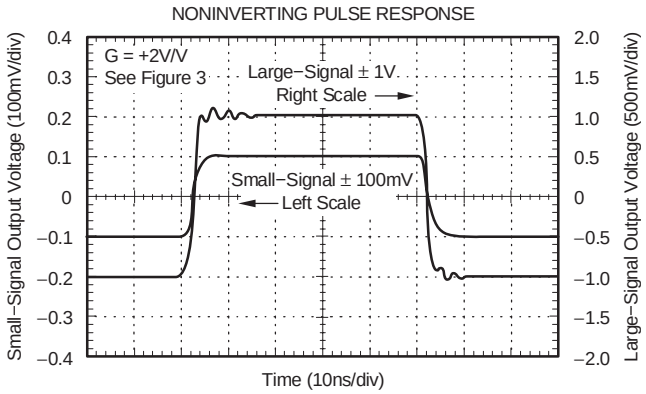
NONINVERTING LARGE−SIGNAL FREQUENCY RESPONSE



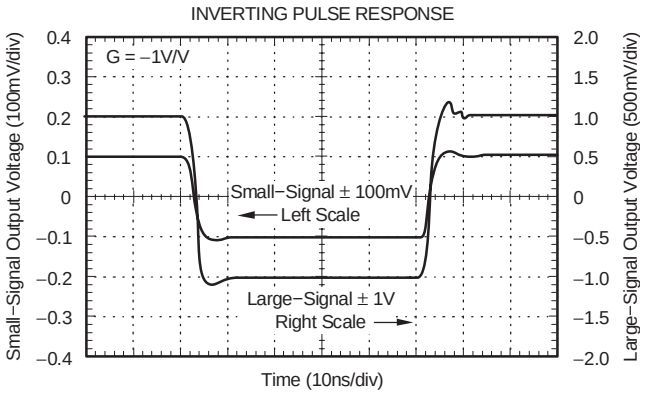
INVERTING LARGE−SIGNAL FREQUENCY RESPONSE



NONINVERTING PULSE RESPONSE



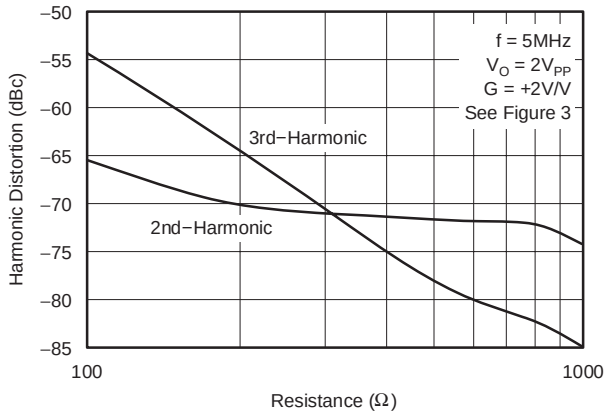
INVERTING PULSE RESPONSE



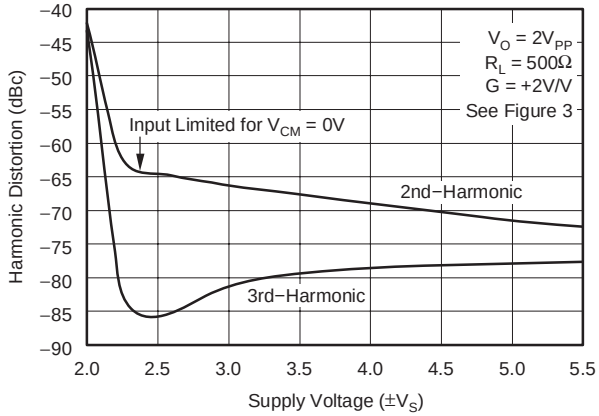
TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = 25°C, G = +2, R_F = 750Ω, and R_L = 150Ω to GND, unless otherwise noted (see Figure 3).

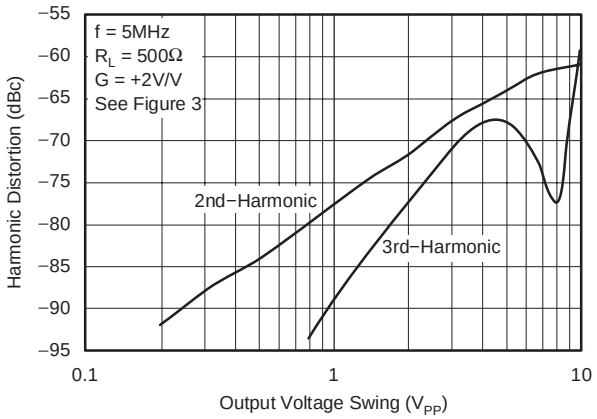
HARMONIC DISTORTION vs LOAD RESISTANCE



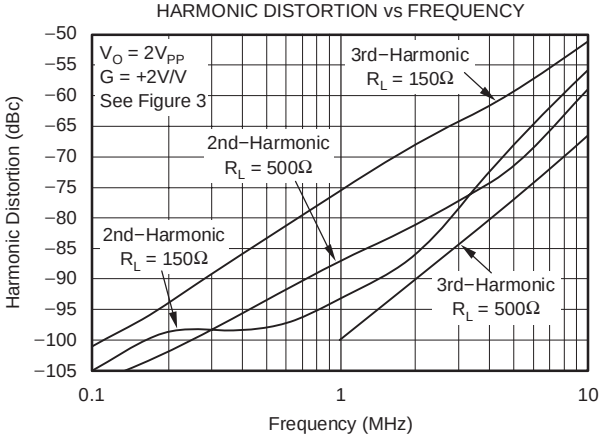
5MHz HARMONIC DISTORTION vs SUPPLY VOLTAGE



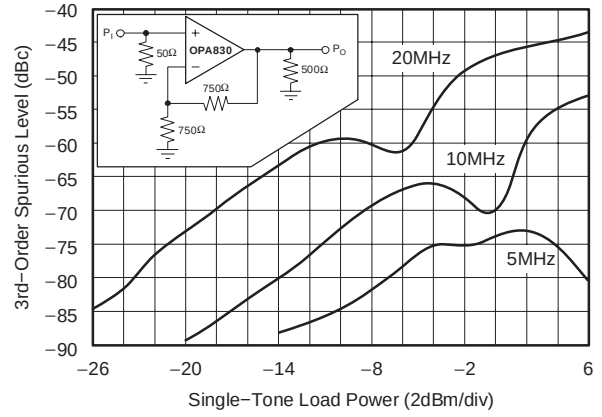
HARMONIC DISTORTION vs OUTPUT VOLTAGE



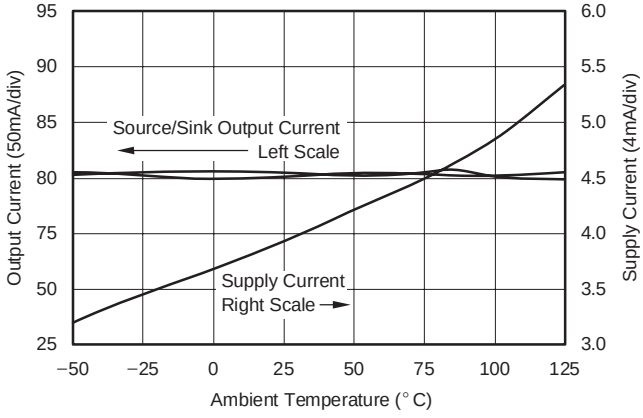
HARMONIC DISTORTION vs FREQUENCY



TWO−TONE, 3RD−ORDER INTERMODULATION SPURIOUS



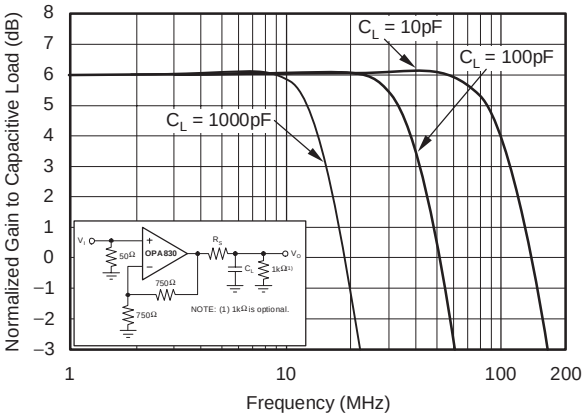
SUPPLY AND OUTPUT CURRENT vs TEMPERATURE



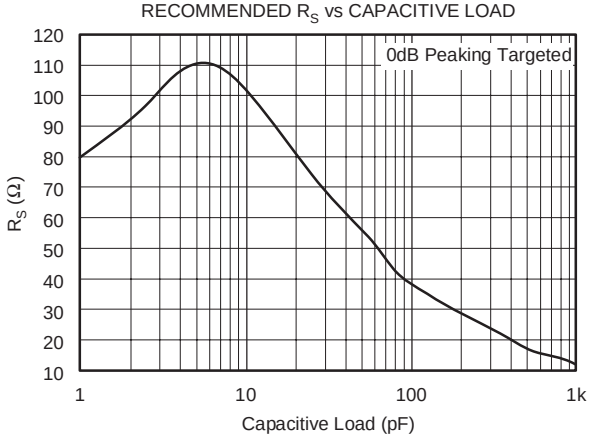
TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = 25°C, G = +2, R_F = 750Ω, and R_L = 150Ω to GND, unless otherwise noted (see Figure 3).

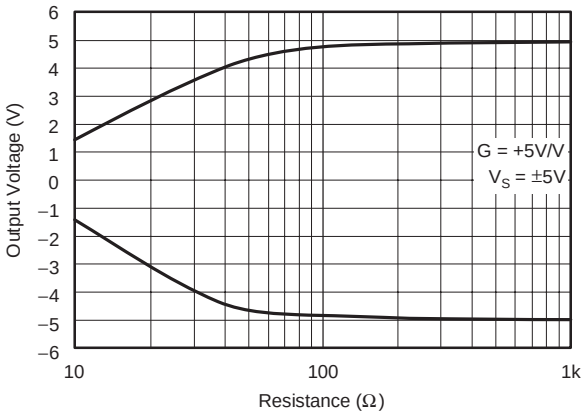
FREQUENCY RESPONSE vs CAPACITIVE LOAD



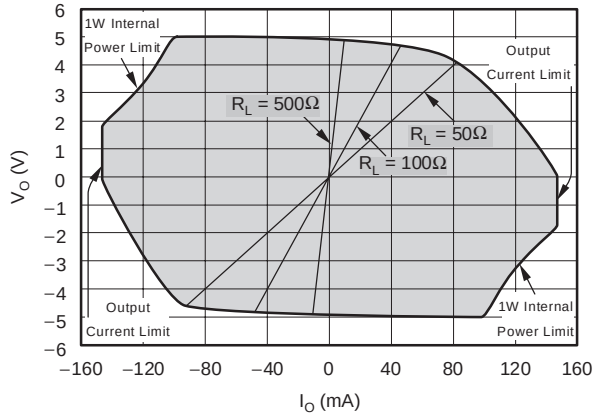
RECOMMENDED R_S vs CAPACITIVE LOAD



OUTPUT SWING vs LOAD RESISTANCE

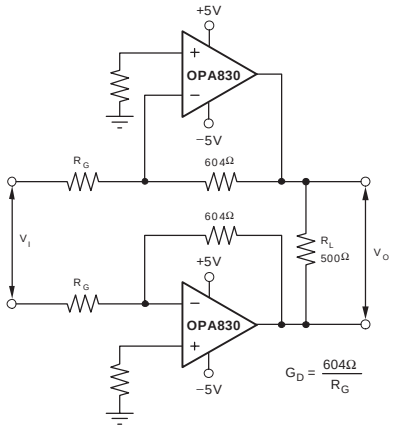


OUTPUT VOLTAGE AND CURRENT LIMITATIONS

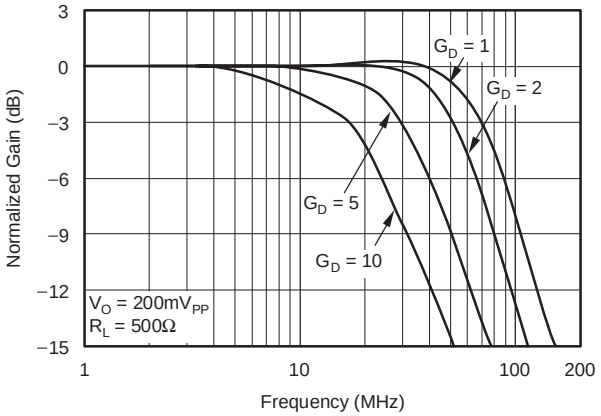


TYPICAL CHARACTERISTICS: $V_S = \pm 5V$, Differential Configuration

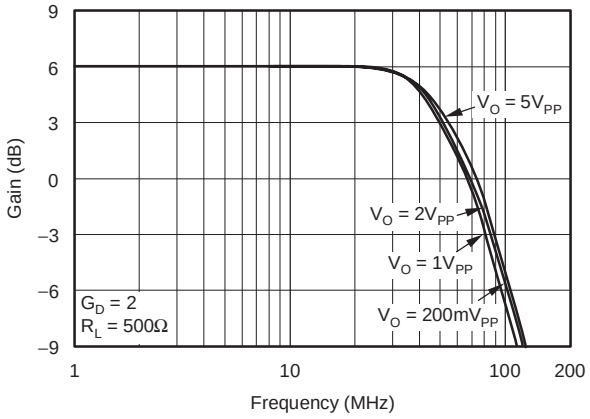
At $T_A = 25°C$, $G_D = +2$, $R_F = 604\Omega$, and $R_L = 500\Omega$, unless otherwise noted.



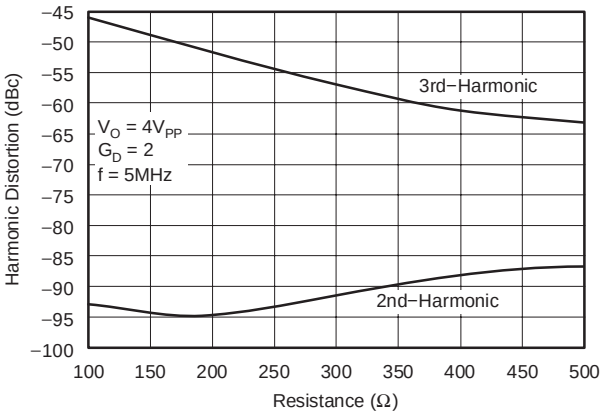
DIFFERENTIAL SMALL−SIGNAL FREQUENCY RESPONSE



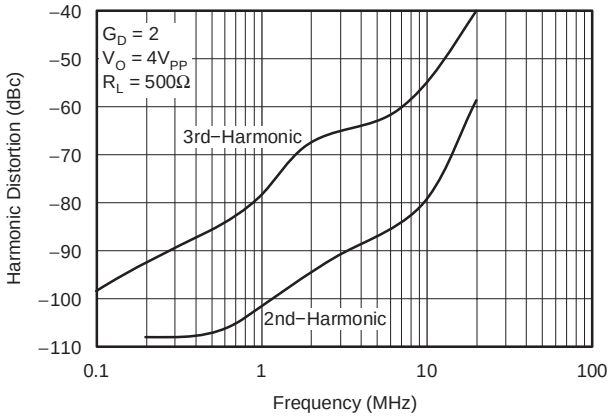
DIFFERENTIAL LARGE−SIGNAL FREQUENCY RESPONSE



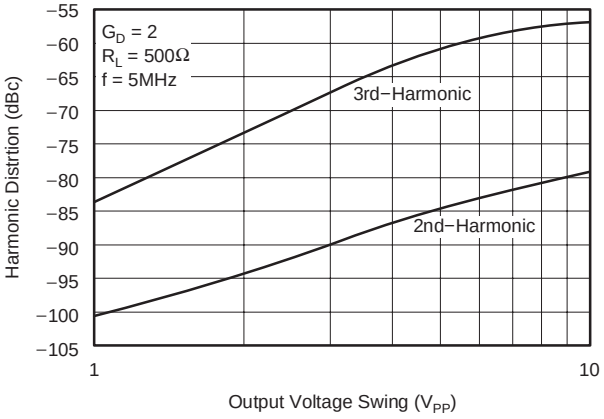
DIFFERENTIAL DISTORTION vs LOAD RESISTANCE



DIFFERENTIAL DISTORTION vs FREQUENCY



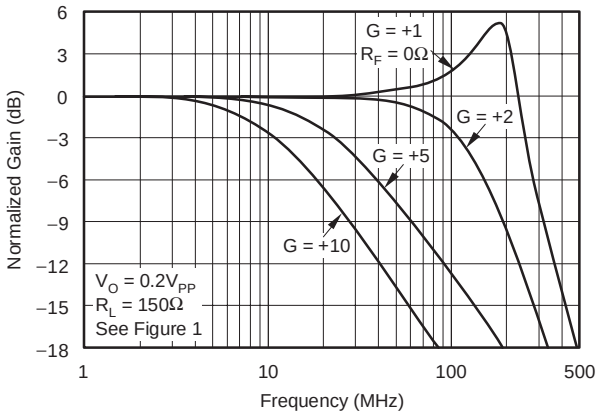
DIFFERENTIAL DISTORTION vs OUTPUT VOLTAGE



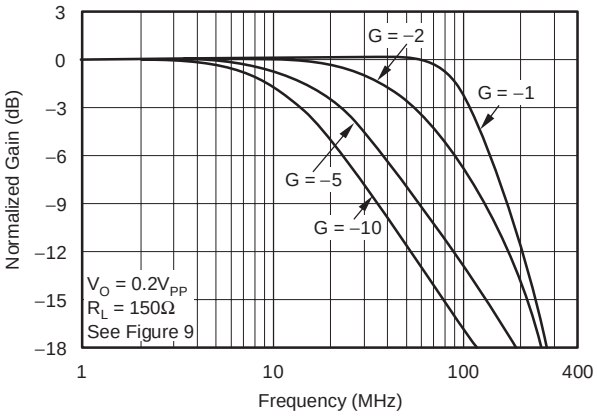
TYPICAL CHARACTERISTICS: V_S = +5V

At T_A = 25°C, G = +2, R_F = 750Ω, R_L = 150Ω to V_S/2, and input V_{CM} = 2.5V, unless otherwise noted (see Figure 1).

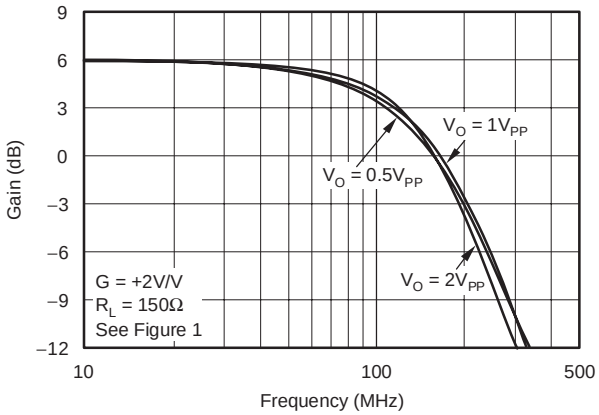
NONINVERTING SMALL−SIGNAL FREQUENCY RESPONSE



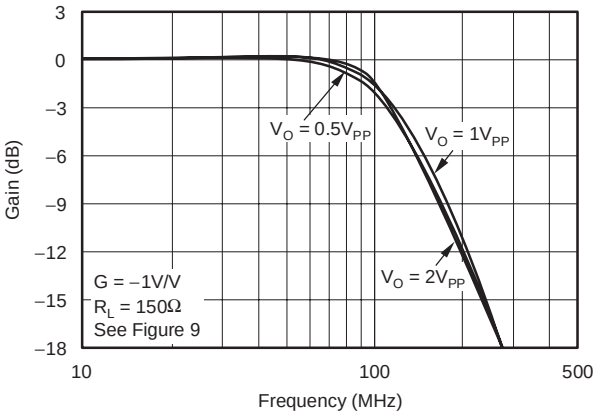
INVERTING SMALL−SIGNAL FREQUENCY RESPONSE



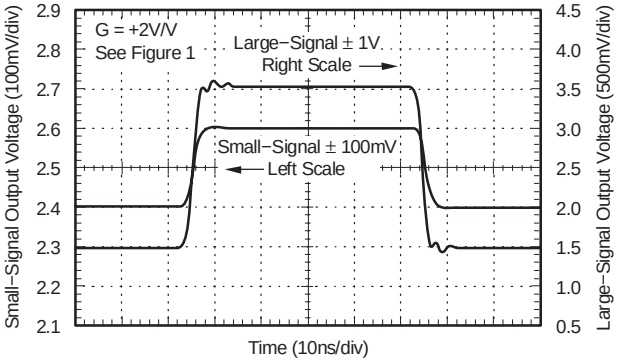
NONINVERTING LARGE−SIGNAL FREQUENCY RESPONSE



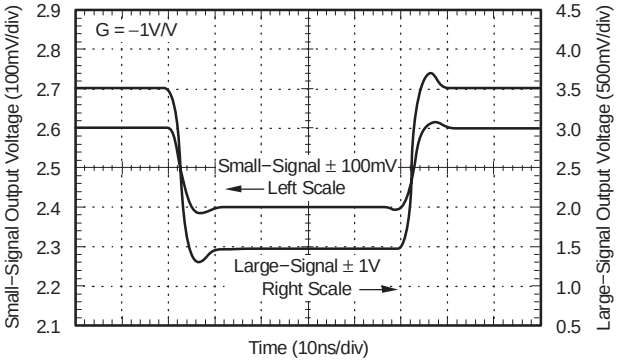
INVERTING LARGE−SIGNAL FREQUENCY RESPONSE



NONINVERTING PULSE RESPONSE



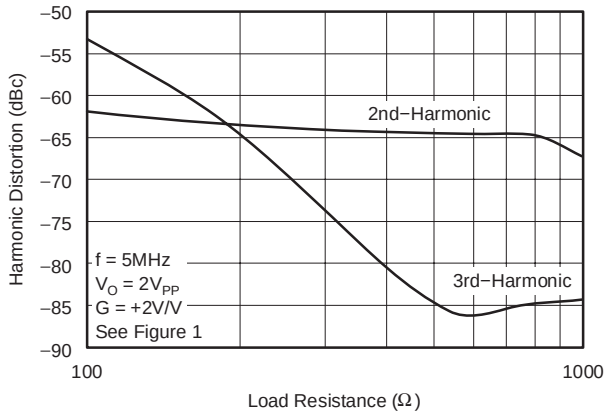
INVERTING PULSE RESPONSE



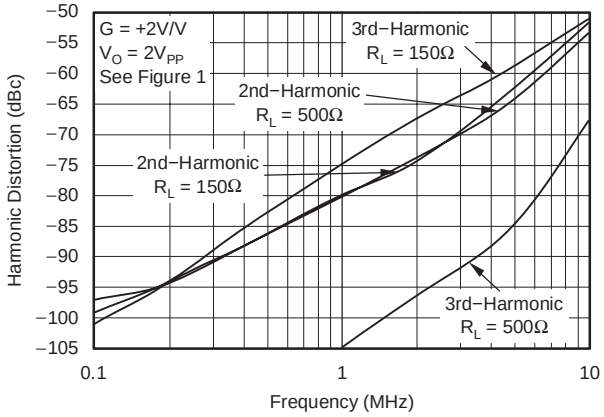
TYPICAL CHARACTERISTICS: V_S = +5V (continued)

At T_A = 25°C, G = +2, R_F = 750Ω, R_L = 150Ω to V_S/2, and input V_{CM} = 2.5V, unless otherwise noted (see Figure 1).

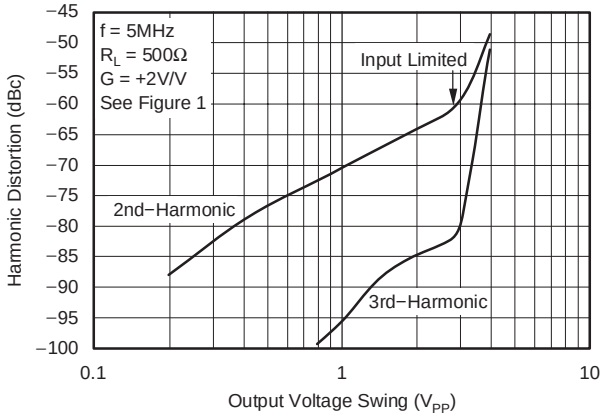
HARMONIC DISTORTION vs LOAD RESISTANCE



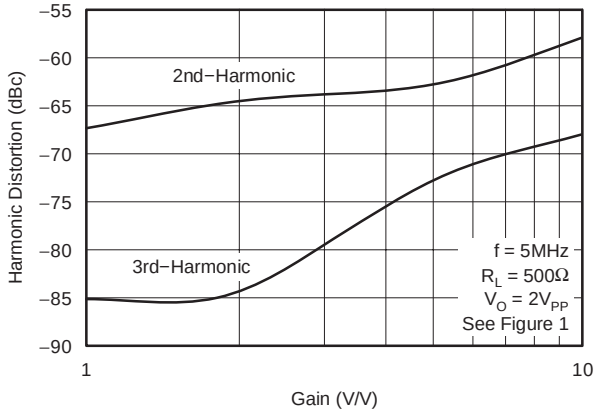
HARMONIC DISTORTION vs FREQUENCY



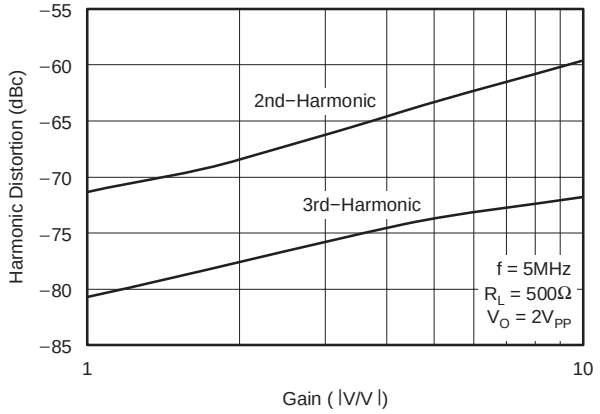
HARMONIC DISTORTION vs OUTPUT VOLTAGE



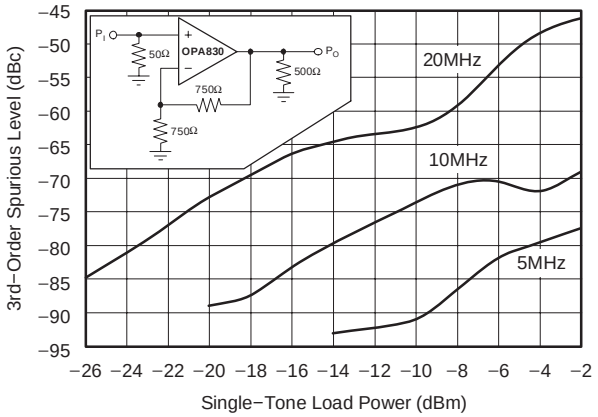
HARMONIC DISTORTION vs NONINVERTING GAIN



HARMONIC DISTORTION vs INVERTING GAIN



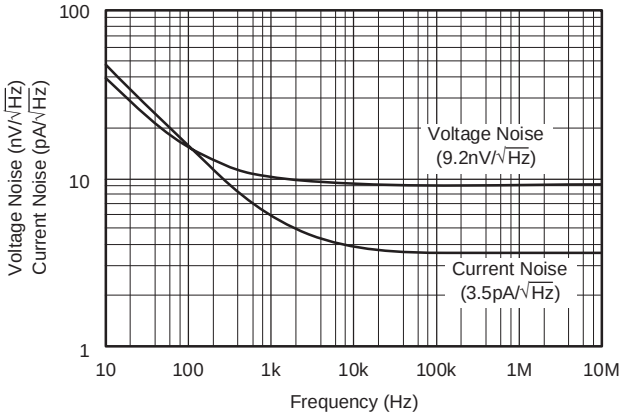
TWO−TONE, 3RD−ORDER INTERMODULATION SPURIOUS



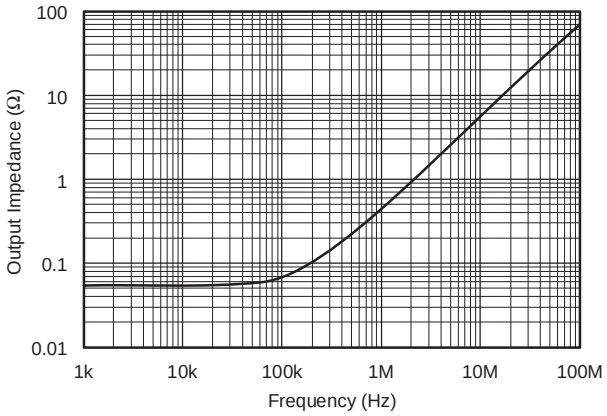
TYPICAL CHARACTERISTICS: V_S = +5V (continued)

At T_A = 25°C, G = +2, R_F = 750Ω, R_L = 150Ω to V_S/2, and input V_{CM} = 2.5V, unless otherwise noted (see Figure 1).

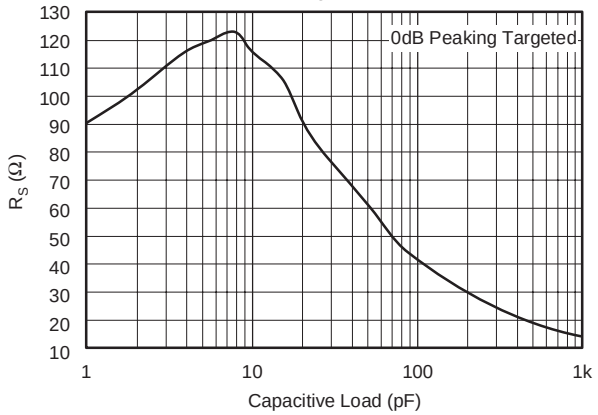
INPUT VOLTAGE AND CURRENT NOISE DENSITY



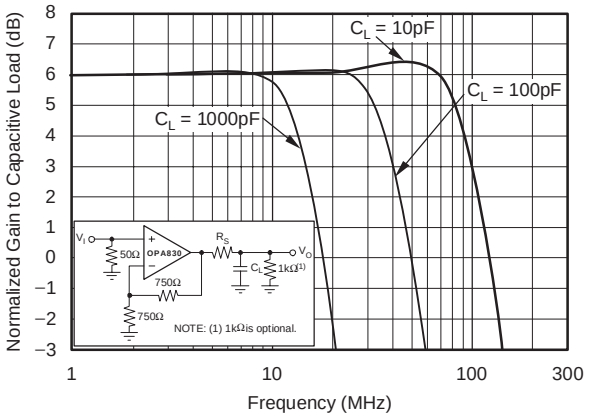
CLOSED−LOOP OUTPUT IMPEDANCE vs FREQUENCY



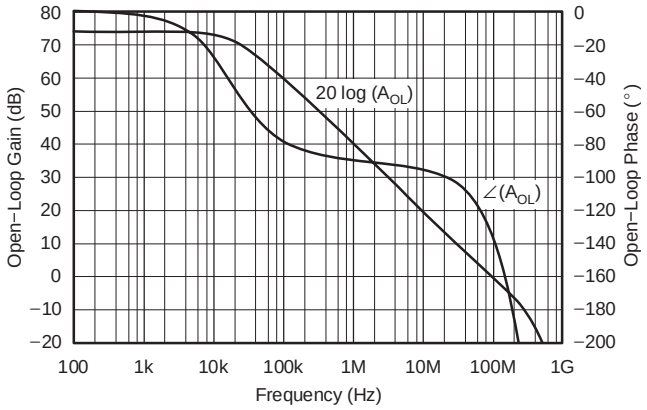
RECOMMENDED R_S vs CAPACITIVE LOAD



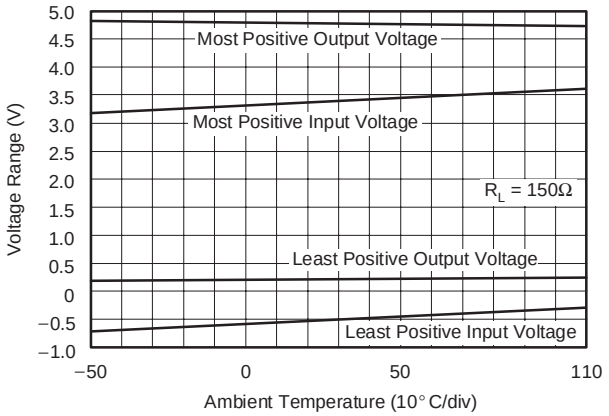
FREQUENCY RESPONSE vs CAPACITIVE LOAD



OPEN−LOOP GAIN AND PHASE



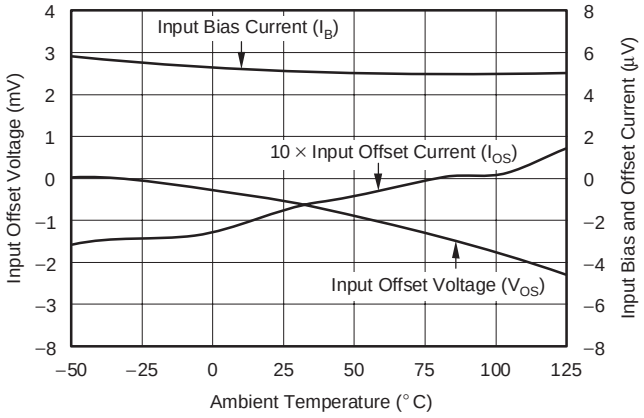
VOLTAGE RANGES vs TEMPERATURE



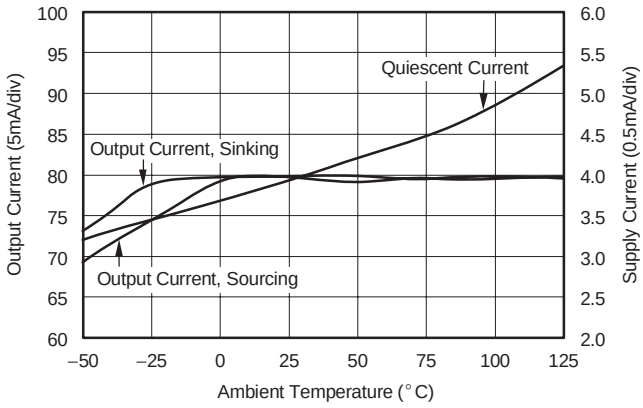
TYPICAL CHARACTERISTICS: V_S = +5V (continued)

At T_A = 25°C, G = +2, R_F = 750Ω, R_L = 150Ω to V_S/2, and input V_{CM} = 2.5V, unless otherwise noted (see Figure 1).

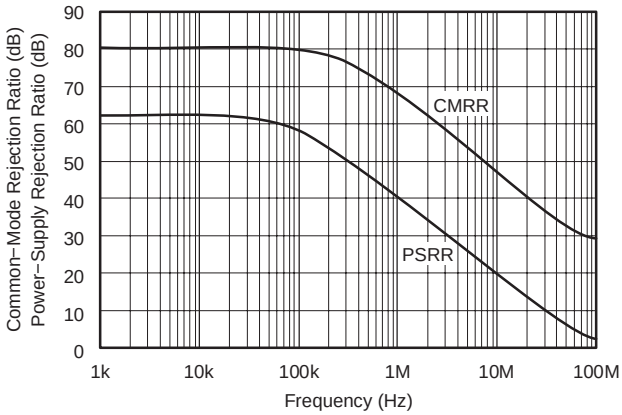
TYPICAL DC DRIFT OVER TEMPERATURE



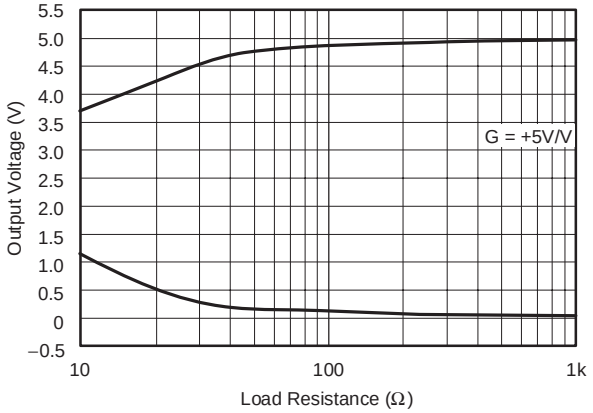
SUPPLY AND OUTPUT CURRENT vs TEMPERATURE



CMRR AND PSRR vs FREQUENCY

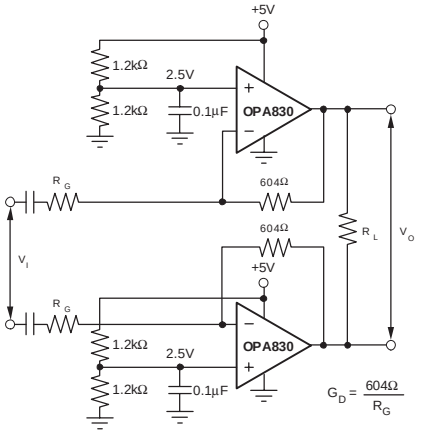


OUTPUT SWING vs LOAD RESISTANCE

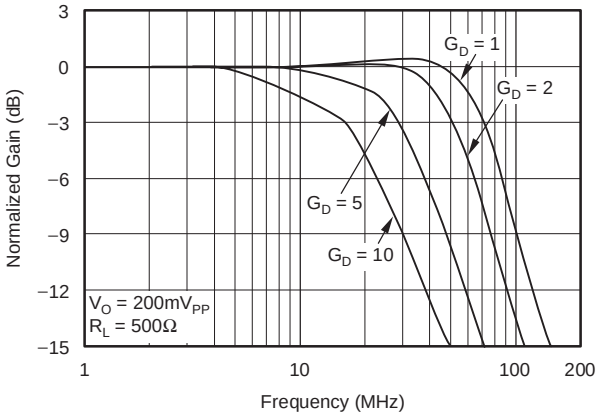


TYPICAL CHARACTERISTICS: V_S = +5V, Differential Configuration

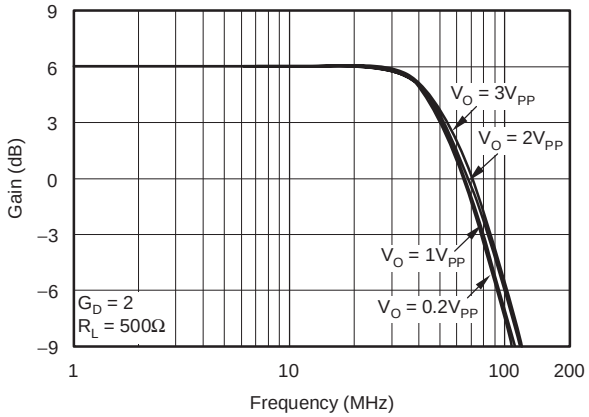
At T_A = 25°C, G = +2, R_F = 604Ω, and R_L = 500Ω differential, unless otherwise noted.



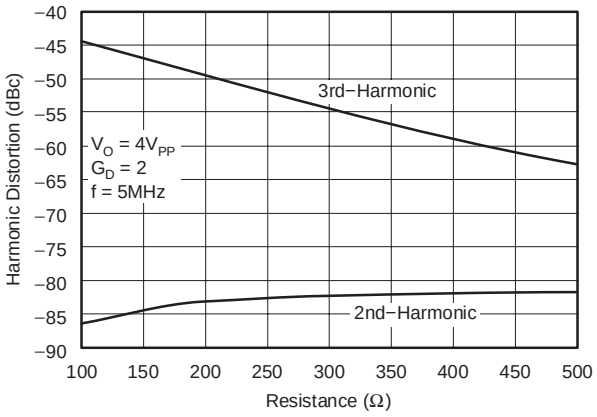
DIFFERENTIAL SMALL−SIGNAL FREQUENCY RESPONSE



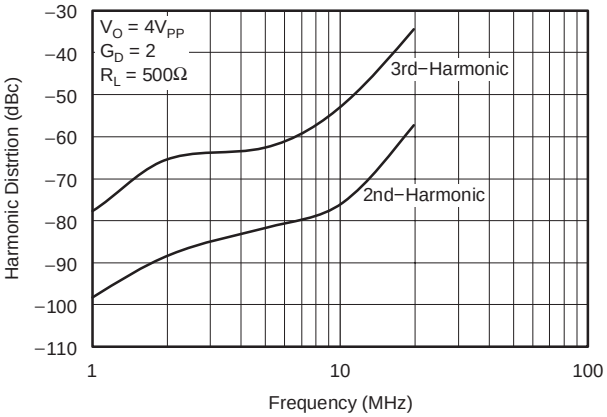
DIFFERENTIAL LARGE−SIGNAL FREQUENCY RESPONSE



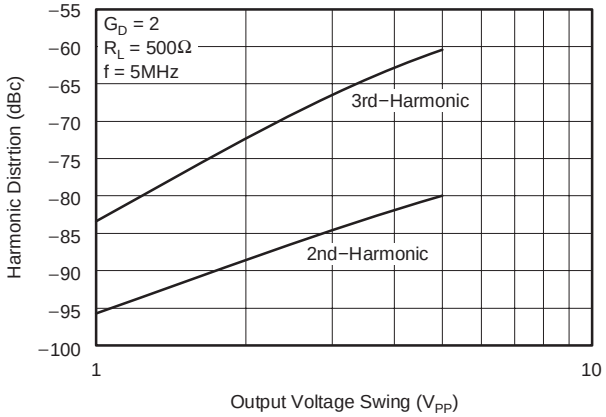
DIFFERENTIAL DISTORTION vs LOAD RESISTANCE



DIFFERENTIAL DISTORTION vs FREQUENCY



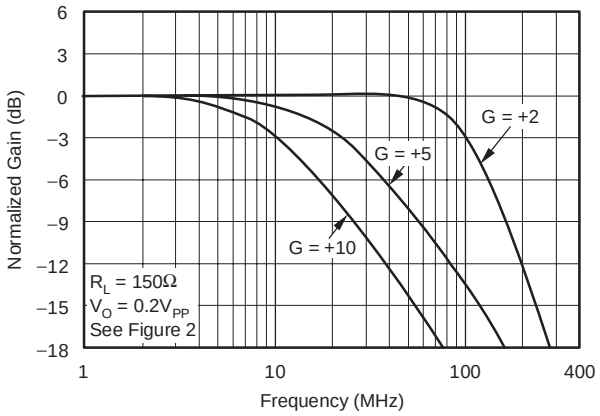
DIFFERENTIAL DISTORTION vs OUTPUT VOLTAGE



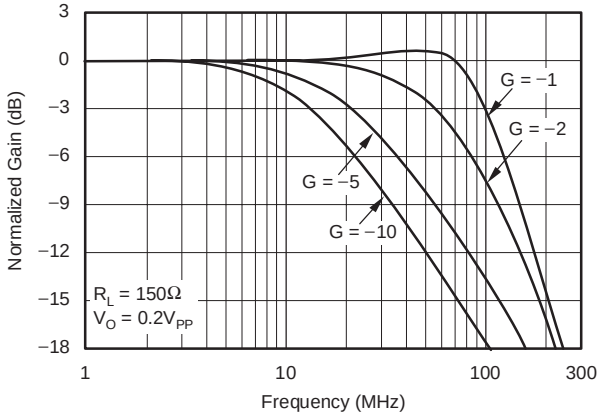
TYPICAL CHARACTERISTICS: V_S = +3V

At T_A = 25°C, G = +2, and R_L = 150Ω to V_S/3, unless otherwise noted (see Figure 2).

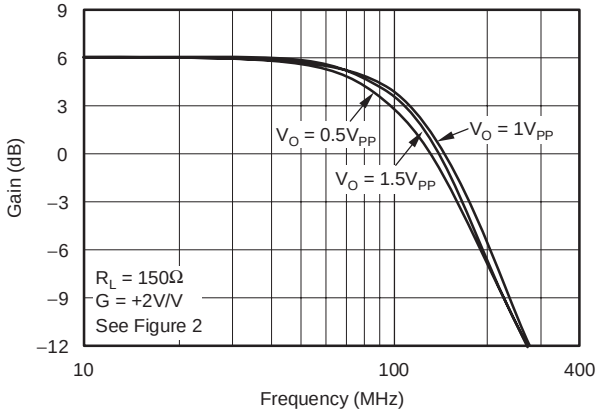
NONINVERTING SMALL−SIGNAL FREQUENCY RESPONSE



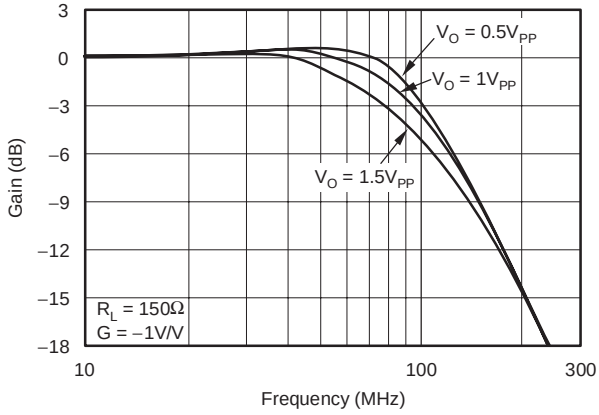
INVERTING SMALL−SIGNAL FREQUENCY RESPONSE



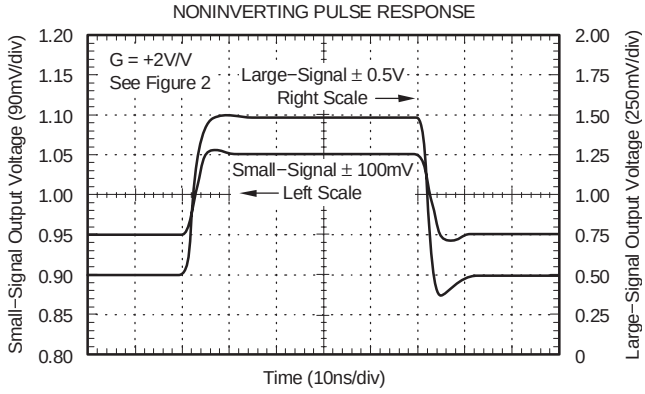
NONINVERTING LARGE−SIGNAL FREQUENCY RESPONSE



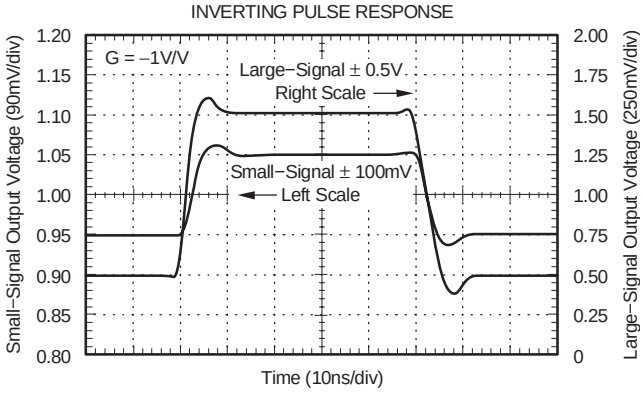
INVERTING LARGE−SIGNAL FREQUENCY RESPONSE



NONINVERTING PULSE RESPONSE



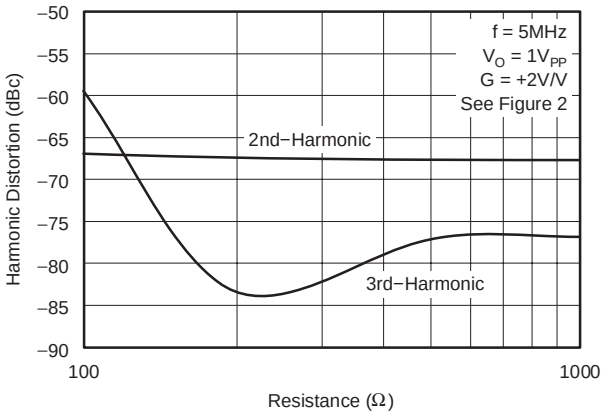
INVERTING PULSE RESPONSE



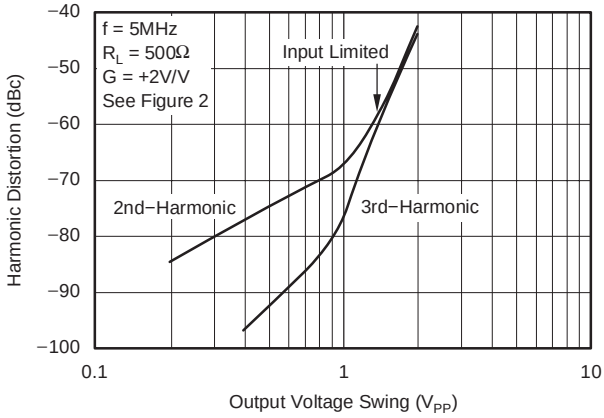
TYPICAL CHARACTERISTICS: V_S = +3V (continued)

At T_A = 25°C, G = +2, and R_L = 150Ω to V_S/3, unless otherwise noted (see Figure 2).

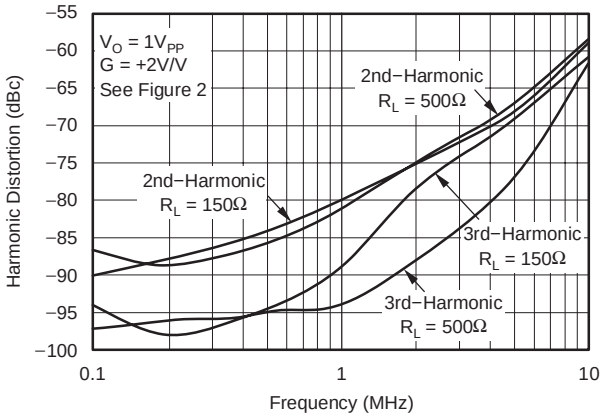
HARMONIC DISTORTION vs LOAD RESISTANCE



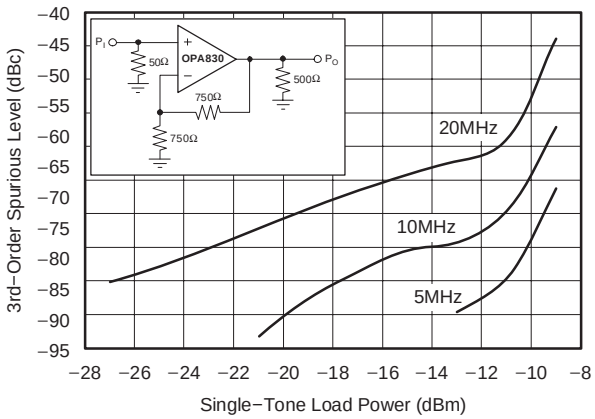
HARMONIC DISTORTION vs OUTPUT VOLTAGE



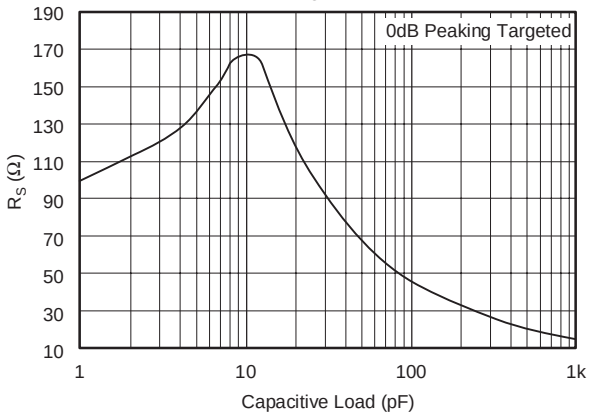
HARMONIC DISTORTION vs FREQUENCY



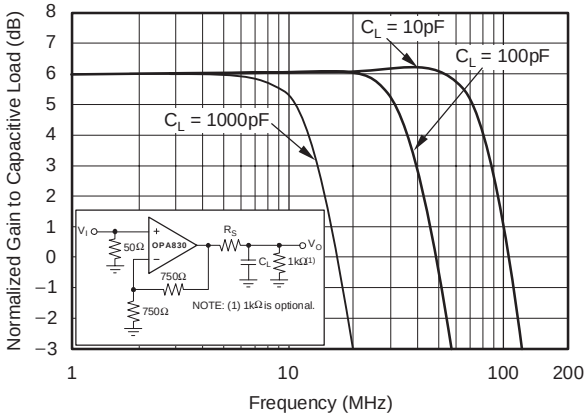
TWO−TONE, 3RD−ORDER INTERMODULATION SPURIOUS



RECOMMENDED R_S vs CAPACITIVE LOAD



FREQUENCY RESPONSE vs CAPACITIVE LOAD



TYPICAL CHARACTERISTICS: V_S = +3V (continued)

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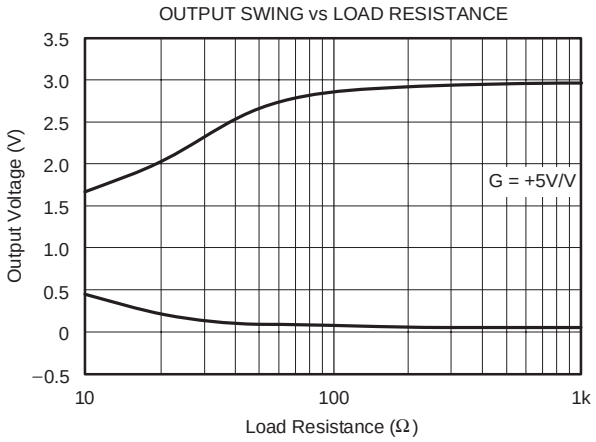

TYPICAL CHARACTERISTICS: V_S = +3V, Differential Configuration

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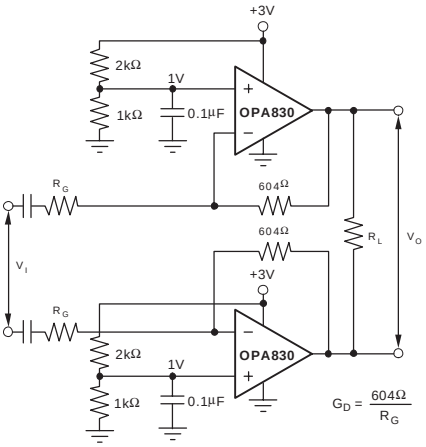
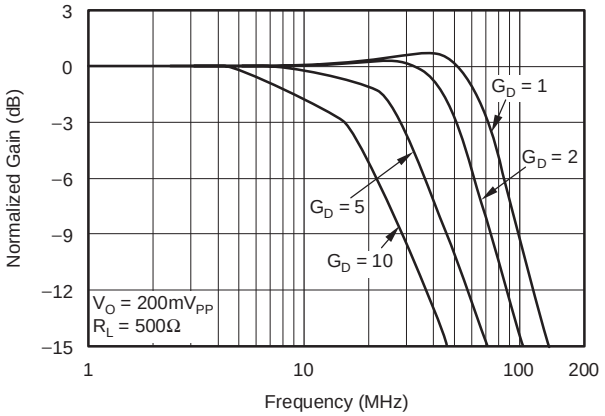
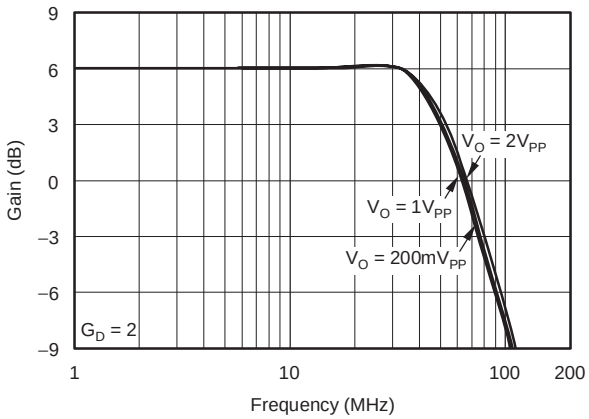


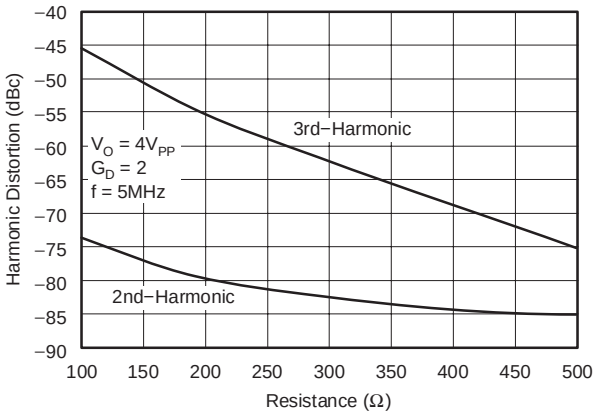
DIFFERENTIAL SMALL−SIGNAL FREQUENCY RESPONSE



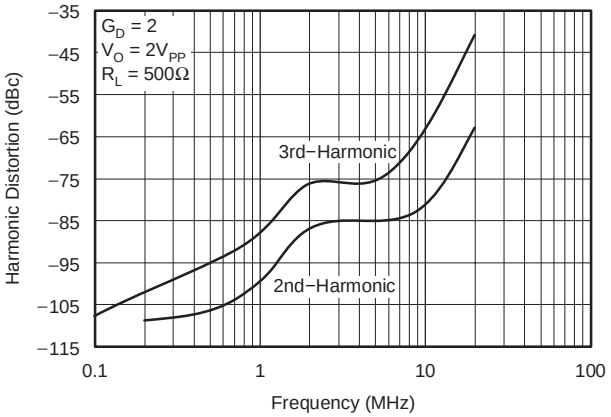
DIFFERENTIAL LARGE−SIGNAL FREQUENCY RESPONSE



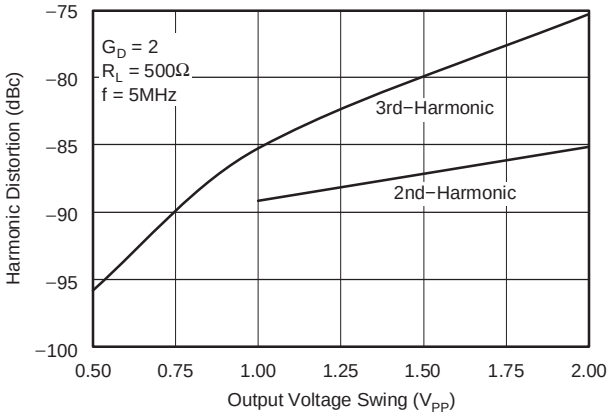
DIFFERENTIAL DISTORTION vs LOAD RESISTANCE



DIFFERENTIAL DISTORTION vs FREQUENCY



DIFFERENTIAL DISTORTION vs OUTPUT VOLTAGE



APPLICATIONS INFORMATION

WIDEBAND VOLTAGE-FEEDBACK OPERATION

The OPA830 is a unity-gain stable, very high-speed voltage-feedback op amp designed for single-supply operation (+3V to +10V). The input stage supports input voltages below ground and to within 1.7V of the positive supply. The complementary common-emitter output stage provides an output swing to within 25mV of ground and the positive supply. The OPA830 is compensated to provide stable operation with a wide range of resistive loads.

Figure 1 shows the AC-coupled, gain of +2 configuration used for the +5V Specifications and Typical Characteristic Curves. For test purposes, the input impedance is set to 50Ω with a resistor to ground. Voltage swings reported in the Electrical Characteristics are taken directly at the input and output pins. For the circuit of Figure 1, the total effective load on the output at high frequencies is 150Ω || 1500Ω. The 1.5kΩ resistors at the noninverting input provide the common-mode bias voltage. Their parallel combination equals the DC resistance at the inverting input (R_F), reducing the DC output offset due to input bias current.

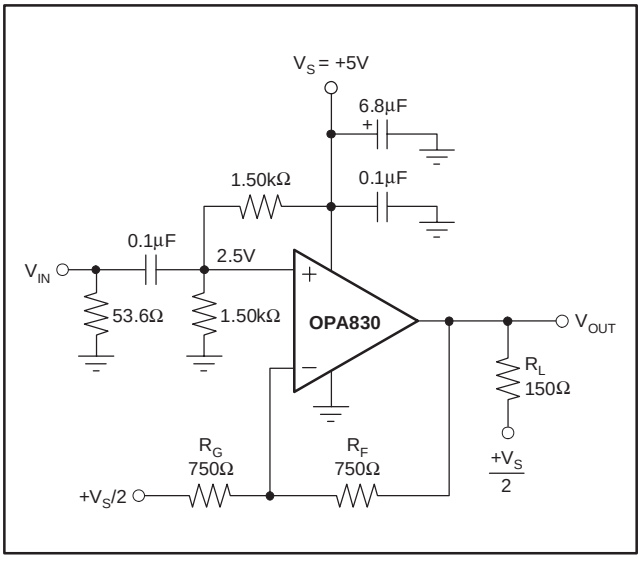


Figure 1. AC-Coupled, G = +2, +5V Single-Supply Specification and Test Circuit

Figure 2 shows the AC-coupled, gain of +2 configuration used for the +3V Specifications and Typical Characteristic Curves. For test purposes, the input impedance is set to 50Ω with a resistor to ground. Voltage swings reported in the Electrical Characteristics are taken directly at the input and output pins. For the circuit of Figure 2, the total effective load on the output at high frequencies is 150Ω || 1500Ω. The 1.13kΩ and 2.26kΩ resistors at the noninverting input provide the common-mode bias voltage. Their parallel combination equals the DC resistance at the inverting input (R_F), reducing the DC output offset due to input bias current.

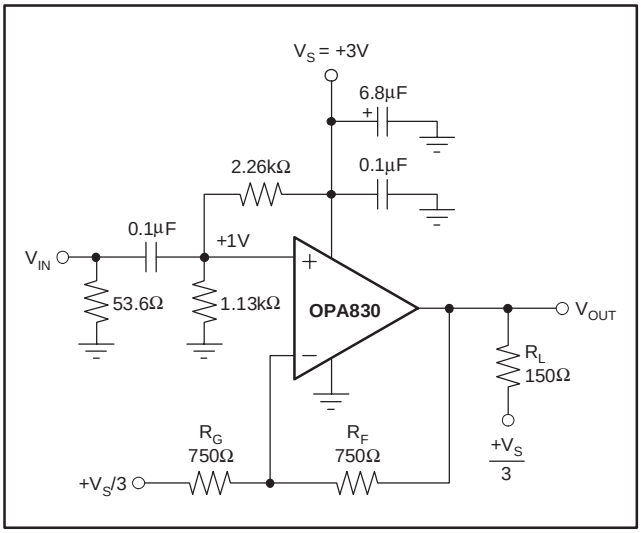


Figure 2. AC-Coupled, G = +2, +3V Single-Supply Specification and Test Circuit

Figure 3 shows the DC-coupled, gain of +2, dual power-supply circuit configuration used as the basis of the ±5V Electrical Characteristics and Typical Characteristics. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 150Ω with a series output resistor. Voltage swings reported in the specifications are taken directly at the input and output pins. For the circuit of Figure 3, the total effective load will be 150Ω || 1.5kΩ. Two optional components are included in Figure 3. An additional resistor (348Ω) is included in series with the noninverting input. Combined with the 25Ω DC source resistance looking back towards the signal generator, this gives an input bias current cancelling resistance that matches the 375Ω source resistance seen at the inverting input (see the ***DC Accuracy and Offset Control*** section). In addition to the usual power-supply decoupling capacitors to ground, a 0.01µF capacitor is included between the two power-supply pins. In practical PC board layouts, this optional capacitor will typically improve the 2nd-harmonic distortion performance by 3dB to 6dB.

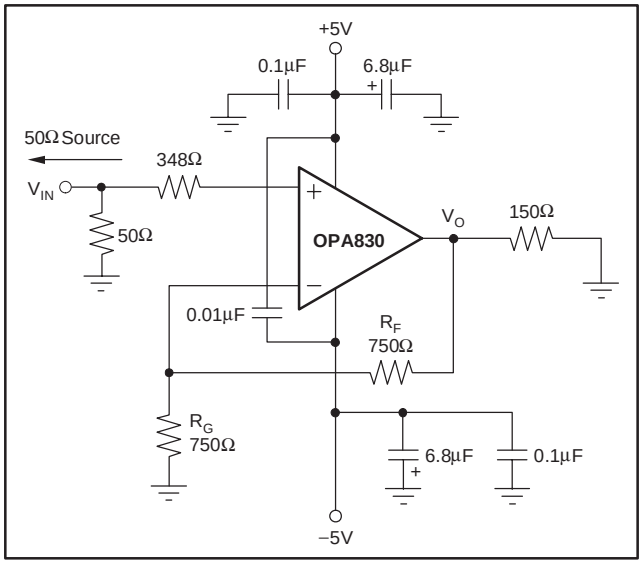


Figure 3. DC-Coupled, G = +2, Bipolar Supply Specification and Test Circuit

SINGLE-SUPPLY ADC INTERFACE

The ADC interface on the front page shows a DC-coupled, single-supply ADC driver circuit. Many systems are now requiring +3V supply capability of both the ADC and its driver. The OPA830 provides excellent performance in this demanding application. Its large input and output voltage ranges and low distortion support converters such as the THS1040 shown in the figure on page 1. The input level-shifting circuitry was designed so that V_{IN} can be between 0V and 0.5V, while delivering an output voltage of 1V to 2V for the THS1040.

DC LEVEL-SHIFTING

Figure 4 shows a DC-coupled noninverting amplifier that level-shifts the input up to accommodate the desired output voltage range. Given the desired signal gain (G), and the amount V_{OUT} needs to be shifted up (ΔV_{OUT}) when V_{IN} is at the center of its range, the following equations give the resistor values that produce the desired performance. Assume that R_4 is between 200Ω and 1.5kΩ.

$NG = G + V_{OUT}/V_S$

$R_1 = R_4/G$

$R_2 = R_4/(NG - G)$

$R_3 = R_4/(NG - 1)$

where:

$NG = 1 + R_4/R_3$

$V_{OUT} = (G)V_{IN} + (NG - G)V_S$

Make sure that V_{IN} and V_{OUT} stay within the specified input and output voltage ranges.

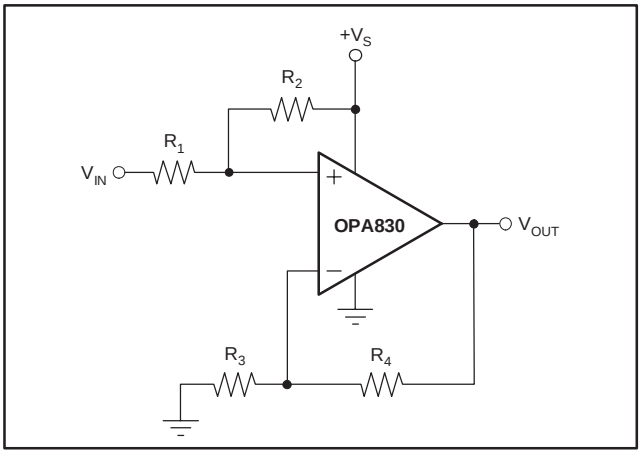


Figure 4. DC Level-Shifting

The circuit on the front page is a good example of this type of application. It was designed to take V_{IN} between 0V and 0.5V and produce V_{OUT} between 1V and 2V when using a +3V supply. This means G = 2.00, and $\Delta V_{OUT} = 1.50V - G \times 0.25V = 1.00V$. Plugging these values into the above equations (with $R_4 = 750\Omega$) gives: NG = 2.33, $R_1 = 375\Omega$, $R_2 = 2.25k\Omega$, and $R_3 = 563\Omega$. The resistors were changed to the nearest standard values for the front page circuit.

AC-COUPLED OUTPUT VIDEO LINE DRIVER

Low-power and low-cost video line drivers often buffer digital-to-analog converter (DAC) outputs with a gain of 2 into a doubly-terminated line. Those interfaces typically require a DC blocking capacitor. For a simple solution, that interface often has used a very large value blocking capacitor (220µF) to limit tilt, or SAG, across the frames. One approach to creating a very low high-pass pole location using much lower capacitor values is shown in Figure 5. This circuit gives a voltage gain of 2 at the output pin with a high-pass pole at 8Hz. Given the 150Ω load, a simple blocking capacitor approach would require a 133µF value. The two much lower valued capacitors give this same low-pass pole using this simple *SAG correction* circuit of Figure 5.

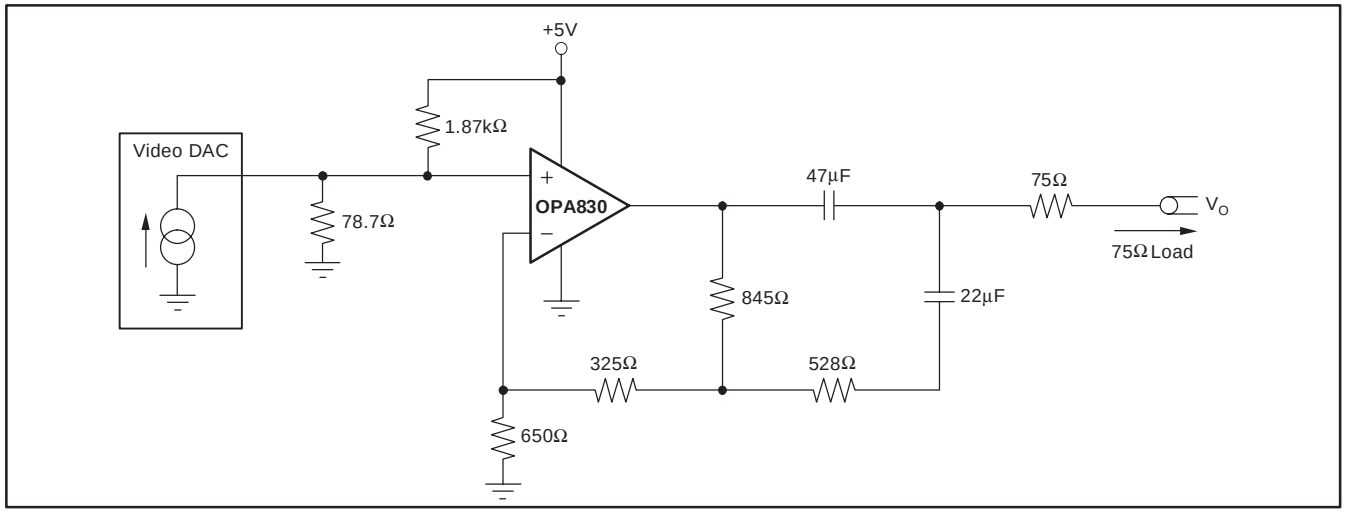


Figure 5. Video Line Driver with SAG Correction

The input is shifted slightly positive in Figure 5 using the voltage divider from the positive supply. This gives about a 200mV input DC offset that will show up at the output pin as a 400mV DC offset when the DAC output is at zero current during the sync tip portion of the video signal. This acts to hold the output in its linear operating region. This will pass on any power-supply noise to the output with a gain of approximately −20dB, so good supply decoupling is recommended on the power-supply pin. Figure 6 shows the frequency response for the circuit of Figure 5. This plot shows the 8Hz low-frequency high-pass pole and a high-end cutoff at approximately 100MHz.

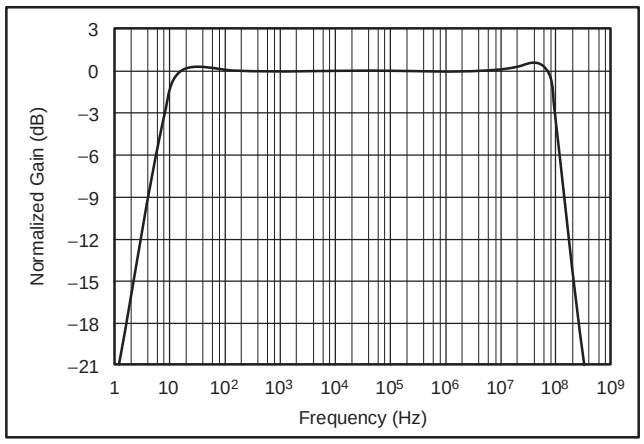


Figure 6. Video Line Driver Response to Matched Load

NONINVERTING AMPLIFIER WITH REDUCED PEAKING

Figure 7 shows a noninverting amplifier that reduces peaking at low gains. The resistor R_C compensates the OPA830 to have higher Noise Gain (NG), which reduces the AC response peaking (typically 5dB at G = +1 without R_C) without changing the DC gain. V_{IN} needs to be a low impedance source, such as an op amp. The resistor values are low to reduce noise. Using both R_T and R_F helps minimize the impact of parasitic impedances.

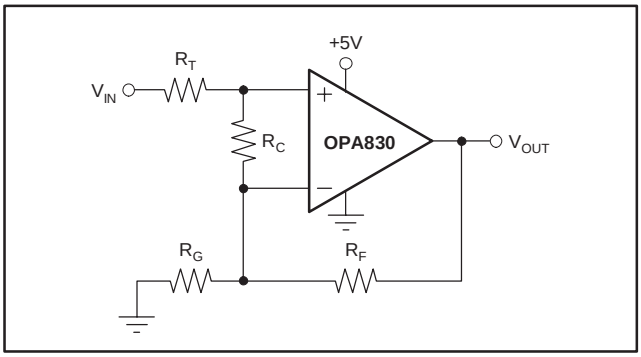


Figure 7. Compensated Noninverting Amplifier

The Noise Gain can be calculated as follows:

$$G_1 = 1 + \frac{R_F}{R_G} \quad (1)$$

$$G_2 = 1 + \frac{R_T + \frac{R_F}{G_1}}{R_C} \quad (2)$$

$$NG = G_1 \times G_2 \quad (3)$$

A unity-gain buffer can be designed by selecting $R_T = R_F = 20.0\Omega$ and $R_C = 40.2\Omega$ (do not use R_G). This gives a noise gain of 2, so the response will be similar to the Characteristics Plots with G = +2. Decreasing R_C to 20.0Ω will increase the noise gain to 3, which typically gives a flat frequency response, but with less bandwidth.

The circuit in Figure 1 can be redesigned to have less peaking by increasing the noise gain to 3. This is accomplished by adding $R_C = 2.55k\Omega$ across the op amp inputs.

SINGLE-SUPPLY ACTIVE FILTER

The OPA830, while operating on a single +3V or +5V supply, lends itself well to high-frequency active filter designs. Again, the key additional requirement is to establish the DC operating point of the signal near the supply midpoint for highest dynamic range. Figure 8 shows an example design of a 1MHz low-pass Butterworth filter using the Sallen-Key topology.

Both the input signal and the gain setting resistor are AC-coupled using 0.1µF blocking capacitors (actually giving bandpass response with the low-frequency pole set to 32kHz for the component values shown). As discussed for Figure 1, this allows the midpoint bias formed by the two 1.87kΩ resistors to appear at both the input and output pins. The midband signal gain is set to +4 (12dB) in this case. The capacitor to ground on the noninverting input is intentionally set larger to dominate input parasitic terms. At a gain of +4, the OPA830 on a single supply will show 30MHz small- and large-signal bandwidth. The resistor values have been slightly adjusted to account for this limited bandwidth in the amplifier stage. Tests of this circuit show a precise 1MHz, −3dB point with a maximally-flat passband (above the 32kHz AC-coupling corner), and a maximum stop band attenuation of 36dB at the amplifier's −3dB bandwidth of 30MHz.

DESIGN-IN TOOLS

DEMONSTRATION BOARDS

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA830 in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in Table 1.

Table 1. Demonstration Fixtures by Package

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA830ID	SO-8	DEM-OPA-SO-1A	SBOU009
OPA830IDBV	SOT23-5	DEM-OPA-SOT-1A	SBOU010

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA830 product folder.

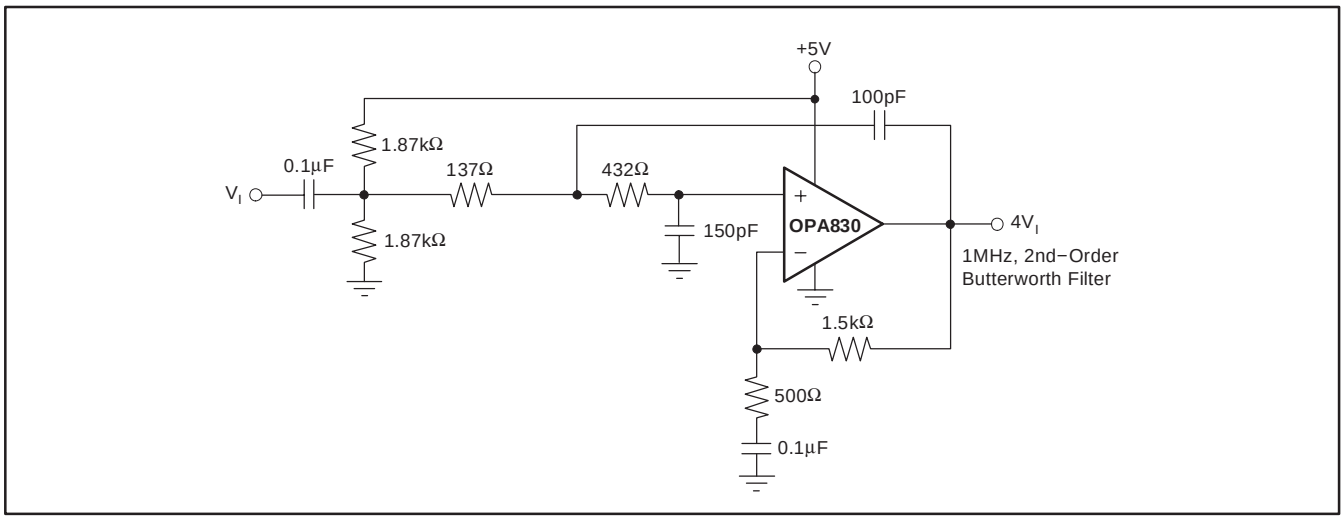


Figure 8. Single-Supply, High-Frequency Active Filter

MACROMODEL AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often a quick way to analyze the performance of the OPA830 and its circuit designs. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can play a major role on circuit performance. A SPICE model for the OPA830 is available through the TI web page (www.ti.com). The applications department is also available for design assistance. These models predict typical small signal AC, transient steps, DC performance, and noise under a wide variety of operating conditions. The models include the noise terms found in the electrical specifications of the data sheet. These models do not attempt to distinguish between the package types in their small-signal AC performance.

OPERATING SUGGESTIONS

OPTIMIZING RESISTOR VALUES

Since the OPA830 is a unity-gain stable, voltage-feedback op amp, a wide range of resistor values may be used for the feedback and gain setting resistors. The primary limits on these values are set by dynamic range (noise and distortion) and parasitic capacitance considerations. For a noninverting unity-gain follower application, the feedback connection should be made with a direct short.

Below 200Ω, the feedback network will present additional output loading which can degrade the harmonic distortion performance of the OPA830. Above 1kΩ, the typical parasitic capacitance (approximately 0.2pF) across the feedback resistor may cause unintentional band limiting in the amplifier response.

A good rule of thumb is to target the parallel combination of R_F and R_G (see Figure 3) to be less than about 400Ω. The combined impedance $R_F \parallel R_G$ interacts with the inverting input capacitance, placing an additional pole in the feedback network, and thus a zero in the forward response. Assuming a 2pF total parasitic on the inverting node, holding $R_F \parallel R_G < 400\Omega$ will keep this pole above 200MHz. By itself, this constraint implies that the feedback resistor R_F can increase to several kΩ at high gains. This is acceptable as long as the pole formed by R_F and any parasitic capacitance appearing in parallel is kept out of the frequency range of interest.

In the inverting configuration, an additional design consideration must be noted. R_G becomes the input resistor and therefore the load impedance to the driving source. If impedance matching is desired, R_G may be set equal to the required termination value. However, at low inverting gains, the resultant feedback resistor value can present a significant load to the amplifier output. For example, an inverting gain of 2 with a 50Ω input matching resistor (= R_G) would require a 100Ω feedback resistor, which would contribute to output loading in parallel with the external load. In such a case, it would be preferable to increase both the R_F and R_G values, and then achieve the input matching impedance with a third resistor to ground (see Figure 9). The total input impedance becomes the parallel combination of R_G and the additional shunt resistor.

BANDWIDTH vs GAIN: NONINVERTING OPERATION

Voltage-feedback op amps exhibit decreasing closed-loop bandwidth as the signal gain is increased. In theory, this relationship is described by the Gain Bandwidth Product (GBP) shown in the specifications. Ideally, dividing GBP by the noninverting signal gain (also called the Noise Gain, or NG) will predict the closed-loop bandwidth. In practice, this only holds true when the phase margin approaches 90°, as it does in high-gain configurations. At low gains (increased feedback factors), most amplifiers will exhibit a more complex response with lower phase margin. The OPA830 is compensated to give a slightly peaked response in a noninverting gain of 2 (see Figure 3). This results in a typical gain of +2 bandwidth of 110MHz, far exceeding that predicted by dividing the 110MHz GBP by 2. Increasing the gain will cause the phase margin to approach 90° and the bandwidth to more closely approach the predicted value of (GBP/NG). At a gain of +10, the 11MHz bandwidth shown in the Electrical Characteristics agrees with that predicted using the simple formula and the typical GBP of 110MHz.

Frequency response in a gain of +2 may be modified to achieve exceptional flatness simply by increasing the noise gain to 3. One way to do this, without affecting the +2 signal gain, is to add an 2.55kΩ resistor across the two inputs, as shown in Figure 7. A similar technique may be used to reduce peaking in unity-gain (voltage follower) applications. For example, by using a 750Ω feedback resistor along with a 750Ω resistor across the two op amp inputs, the voltage follower response will be similar to the gain of +2 response of Figure 2. Further reducing the value of the resistor across the op amp inputs will further dampen the frequency response due to increased noise gain. The OPA830 exhibits minimal bandwidth reduction going to single-supply (+5V) operation as compared with ±5V. This minimal reduction is because the internal bias control circuitry retains nearly constant quiescent current as the total supply voltage between the supply pins is changed.

INVERTING AMPLIFIER OPERATION

All of the familiar op amp application circuits are available with the OPA830 to the designer. See Figure 9 for a typical inverting configuration where the I/O impedances and signal gain from Figure 1 are retained in an inverting circuit configuration. Inverting operation is one of the more common requirements and offers several performance benefits. It also allows the input to be biased at $V_S/2$ without any headroom issues. The output voltage can be independently moved to be within the output voltage range with coupling capacitors, or bias adjustment resistors.

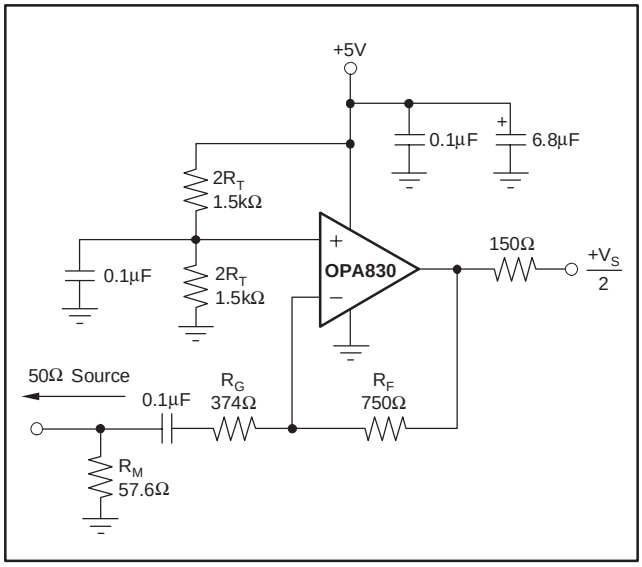


Figure 9. AC-Coupled, G = −2 Example Circuit

In the inverting configuration, three key design considerations must be noted. The first consideration is that the gain resistor (R_G) becomes part of the signal channel input impedance. If input impedance matching is desired (which is beneficial whenever the signal is coupled through a cable, twisted pair, long PC board trace, or other transmission line conductor), R_G may be set equal to the required termination value and R_F adjusted to give the desired gain. This is the simplest approach and results in optimum bandwidth and noise performance.

However, at low inverting gains, the resulting feedback resistor value can present a significant load to the amplifier output. For an inverting gain of 2, setting R_G to 50Ω for input matching eliminates the need for R_M but requires a 100Ω feedback resistor. This configuration has the interesting advantage of the noise gain becoming equal to 2 for a 50Ω source impedance—the same as the noninverting circuits considered above. The amplifier output will now see the 100Ω feedback resistor in parallel with the external load. In general, the feedback resistor should be limited to the 200Ω to 1.5kΩ range. In this case, it is preferable to increase both the R_F and R_G values, as shown in Figure 9, and then achieve the input matching impedance with a third resistor (R_M) to ground. The total input impedance becomes the parallel combination of R_G and R_M.

The second major consideration, touched on in the previous paragraph, is that the signal source impedance becomes part of the noise gain equation and hence influences the bandwidth. For the example in Figure 9, the R_M value combines in parallel with the external 50Ω source impedance (at high frequencies), yielding an effective driving impedance of 50Ω || 57.6Ω = 26.8Ω. This impedance is added in series with R_G for calculating the noise gain. The resulting noise gain is 2.87 for Figure 9, as opposed to only 2 if R_M could be eliminated as discussed above. The bandwidth will therefore be lower for the gain of −2 circuit of Figure 9 (NG = +2.87) than for the gain of +2 circuit of Figure 1.

The third important consideration in inverting amplifier design is setting the bias current cancellation resistors on the noninverting input (a parallel combination of R_T = 750Ω). If this resistor is set equal to the total DC resistance looking out of the inverting node, the output DC error, due to the input bias currents, will be reduced to (Input Offset Current) times R_F. With the DC blocking capacitor in series with R_G, the DC source impedance looking out of the inverting mode is simply R_F = 750Ω for Figure 9. To reduce the additional high-frequency noise introduced by this resistor and power-supply feed-through, R_T is bypassed with a capacitor.

OUTPUT CURRENT AND VOLTAGES

The OPA830 provides outstanding output voltage capability. For the +5V supply, under no-load conditions at +25°C, the output voltage typically swings closer than 90mV to either supply rail.

The minimum specified output voltage and current specifications over temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup will the output current and voltage decrease to the numbers shown in the ensured tables. As the output transistors deliver power, their junction temperatures will increase, decreasing their V_{BE}s (increasing the available output voltage swing) and increasing their current gains (increasing the available output current). In steady-state operation, the available output voltage and current will always be greater than that shown in the over-temperature specifications, since the output stage junction temperatures will be higher than the minimum specified operating ambient.

To maintain maximum output stage linearity, no output short-circuit protection is provided. This will not normally be a problem, since most applications include a series matching resistor at the output that will limit the internal power dissipation if the output side of this resistor is shorted to ground. However, shorting the output pin directly to the adjacent positive power-supply pin (8-pin packages) will, in most cases, destroy the amplifier. If additional short-circuit protection is required, consider a small series resistor in the power-supply leads. This will reduce the available output voltage swing under heavy output loads.

DRIVING CAPACITIVE LOADS

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC—including additional external capacitance which may be recommended to improve ADC linearity. A high-speed, high open-loop gain amplifier like the OPA830 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution

is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load.

The Typical Characteristic curves show the recommended R_S versus capacitive load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA830. Long PC board traces, unmatched cables, and connections to multiple devices can easily exceed this value. Always consider this effect carefully, and add the recommended series resistor as close as possible to the output pin (see the ***Board Layout Guidelines*** section).

The criterion for setting this R_S resistor is a maximum bandwidth, flat frequency response at the load. For a gain of +2, the frequency response at the output pin is already slightly peaked without the capacitive load, requiring relatively high values of R_S to flatten the response at the load. Increasing the noise gain will also reduce the peaking (see Figure 7).

DISTORTION PERFORMANCE

The OPA830 provides good distortion performance into a 150Ω load. Relative to alternative solutions, it provides exceptional performance into lighter loads and/or operating on a single +3V supply. Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd-harmonic will dominate the distortion with a negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network; in the noninverting configuration (see Figure 3) this is sum of $R_F + R_G$, while in the inverting configuration, only R_F needs to be included in parallel with the actual load. Running differential suppresses the 2nd-harmonic, as shown in the differential typical characteristic curves.

NOISE PERFORMANCE

High slew rate, unity-gain stable, voltage-feedback op amps usually achieve their slew rate at the expense of a higher input noise voltage. The 9.2nV/√Hz input voltage noise for the OPA830 however, is much lower than comparable amplifiers. The input-referred voltage noise and the two input-referred current noise terms (2.8pA/√Hz) combine to give low output noise under a wide variety of operating conditions. Figure 10 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

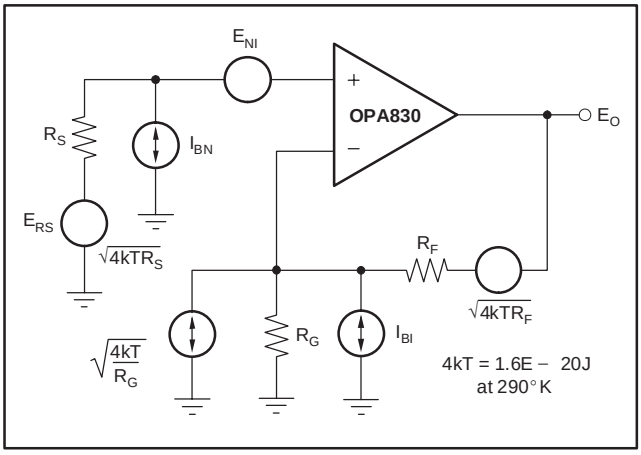


Figure 10. Noise Analysis Model

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 4 shows the general form for the output noise voltage using the terms shown in Figure 10:

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FNG} \quad (4)$$

Dividing this expression by the noise gain ($NG = (1 + R_F/R_G)$) will give the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 5:

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (5)$$

Evaluating these two equations for the circuit and component values shown in Figure 1 will give a total output spot noise voltage of 19.3nV/√Hz and a total equivalent input spot noise voltage of 9.65nV/√Hz. This is including the noise added by the resistors. This total input-referred spot noise voltage is not much higher than the 9.2nV/√Hz specification for the op amp voltage noise alone.

DC ACCURACY AND OFFSET CONTROL

The balanced input stage of a wideband voltage-feedback op amp allows good output DC accuracy in a wide variety of applications. The power-supply current trim for the OPA830 gives even tighter control than comparable products. Although the high-speed input stage does require relatively high input bias current (typically 5μA out of each input terminal), the close matching between them may be used to reduce the output DC error caused by this current. This is done by matching the DC source resistances appearing at the two inputs. Evaluating the configuration of Figure 3 (which has matched DC input

resistances), using worst-case +25°C input offset voltage and current specifications, gives a worst-case output offset voltage equal to:

(NG = noninverting signal gain at DC)

$\pm(NG \times V_{OS(MAX)}) + (R_F \times I_{OS(MAX)})$

$= \pm(2 \times 7mV) \times (375\Omega \times 1\mu A)$

$= \pm 14.38mV$

A fine-scale output offset null, or DC operating point adjustment, is often required. Numerous techniques are available for introducing DC offset control into an op amp circuit. Most of these techniques are based on adding a DC current through the feedback resistor. In selecting an offset trim method, one key consideration is the impact on the desired signal path frequency response. If the signal path is intended to be noninverting, the offset control is best applied as an inverting summing signal to avoid interaction with the signal source. If the signal path is intended to be inverting, applying the offset control to the noninverting input may be considered. Bring the DC offsetting current into the inverting input node through resistor values that are much larger than the signal path resistors. This will insure that the adjustment circuit has minimal effect on the loop gain and hence the frequency response.

THERMAL ANALYSIS

Maximum desired junction temperature will set the maximum allowed internal power dissipation, as described below. In no case should the maximum junction temperature be allowed to exceed 150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load; though, for resistive loads connected to mid-supply ($V_S/2$), P_{DL} is at a maximum when the output is fixed at a voltage equal to $V_S/4$ or $3V_S/4$. Under this condition, $P_{DL} = V_S^2/(16 \times R_L)$, where R_L includes feedback network loading.

Note that it is the power in the output stage, and not into the load, that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA830 (SOT23-5 package) in the circuit of Figure 1 operating at the maximum specified ambient temperature of +85°C and driving a 150Ω load at mid-supply.

$P_D = 10V \times 3.9mA + 5^2/(16 \times (150\Omega \parallel 750\Omega)) = 51.5mW$

Maximum $T_J = +85°C + (0.051W \times 150°C/W) = 93°C$.

Although this is still well below the specified maximum junction temperature, system reliability considerations may require lower ensured junction temperatures. The highest possible internal dissipation will occur if the load requires current to be forced into the output at high output voltages or sourced from the output at low output voltages. This puts a high current through a large internal voltage drop in the output transistors.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier like the OPA830 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power-supply pins to high-frequency 0.1µF decoupling capacitors. At the device pins, the ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Each power-supply connection should always be decoupled with one of these capacitors. An optional supply decoupling capacitor (0.1µF) across the two power supplies (for bipolar operation) will improve 2nd-harmonic distortion performance. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high-frequency performance. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film or carbon composition axially-leaded resistors can also provide good high-frequency performance. Again, keep their leads and PC board traces as short as possible. Never use wire-wound type resistors in a high-frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create

significant time constants that can degrade performance. Good axial metal film or surface-mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values > 1.5kΩ, this parasitic capacitance can add a pole and/or zero below 500MHz that can effect circuit operation. Keep resistor values as low as possible consistent with load driving considerations. The 750Ω feedback used in the Typical Characteristics is a good starting point for design.

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the typical characteristic curve *Recommended R_S vs Capacitive Load*. Low parasitic capacitive loads (< 5pF) may not need an R_S since the OPA830 is nominally compensated to operate with a 2pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary onboard, and in fact, a higher impedance environment will improve distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined (based on board material and trace dimensions), a matching series resistor into the trace from the output of the OPA830 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the typical characteristic curve *Recommended R_S vs Capacitive Load*. This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA830 onto the board.

INPUT AND ESD PROTECTION

The OPA830 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 11.

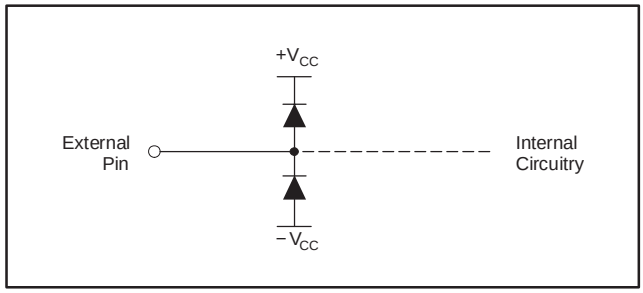


Figure 11. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (that is, in systems with ±15V supply parts driving into the OPA830), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible, since high values degrade both noise performance and frequency response.

Revision History

DATE	REV	PAGE	SECTION	DESCRIPTION
8/07	E	1	Features	Changed 550V/ns to 550V/µs.
3/06	D	1	—	Changed 30MSPS to 40MSPS in front-page graphic.
		2	Absolute Maximum Table	Changed ±1.2V to ±2.5V in third row of Absolute Maximum Ratings table.
		22	Design-In Tools	Changed *Demonstration Boards* section in Design-In Tools, including both paragraphs and Table 1.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
OPA830ID	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA830IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA830IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA830IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA830IDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA830IDG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA830IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA830IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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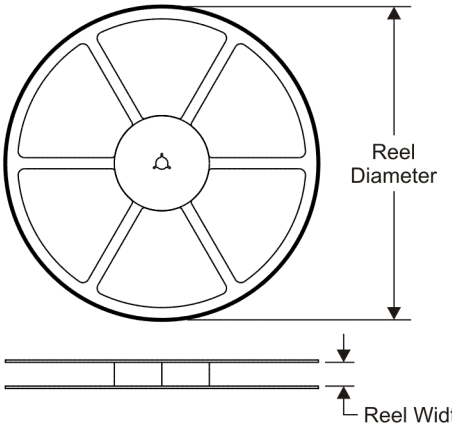
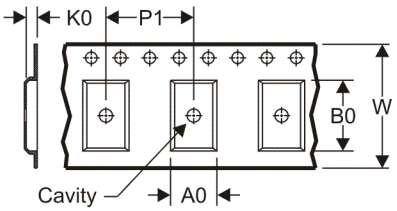
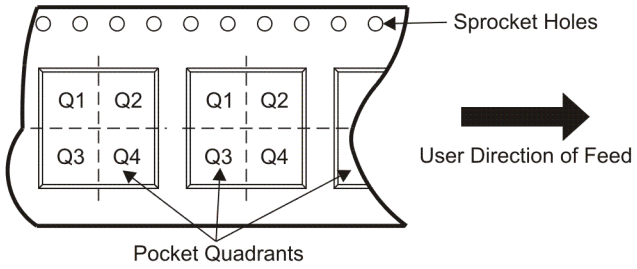


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

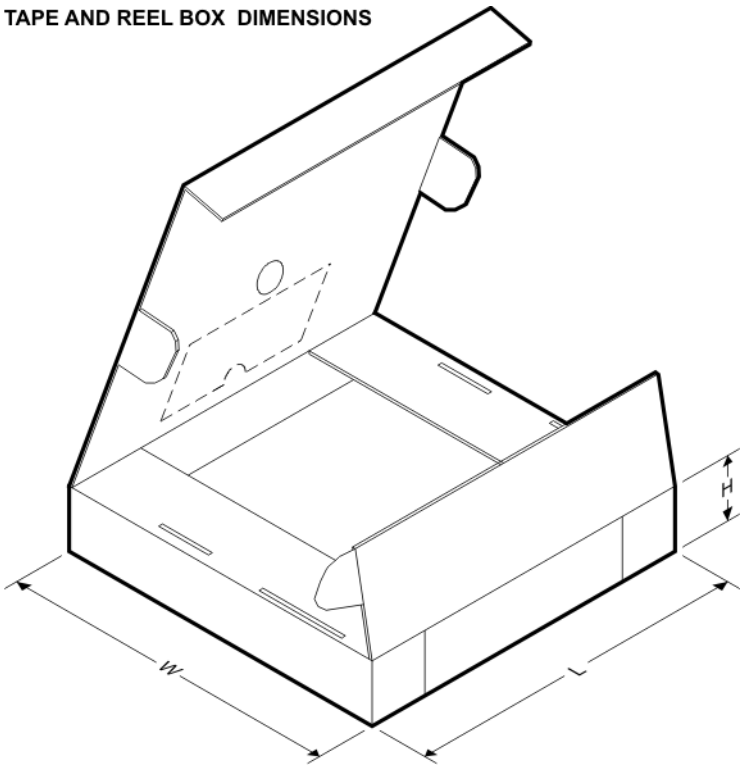
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA830IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.1	1.39	4.0	8.0	Q3
OPA830IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.1	1.39	4.0	8.0	Q3
OPA830IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

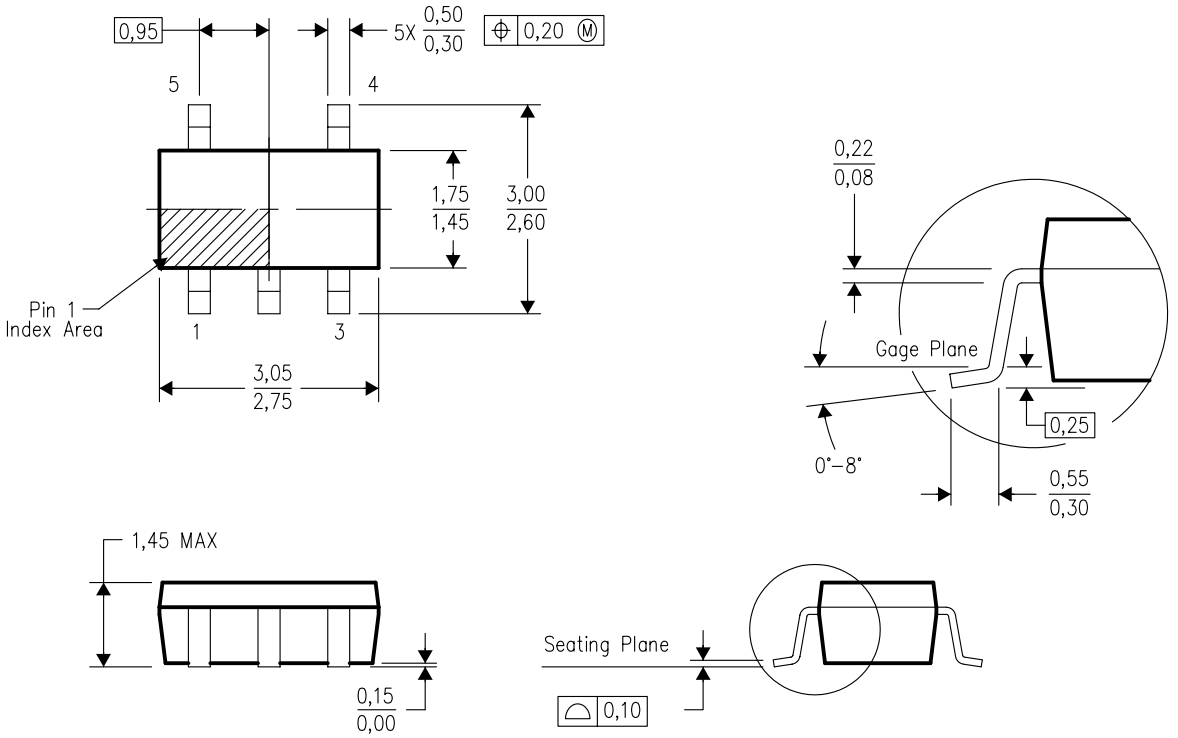
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA830IDBVR	SOT-23	DBV	5	3000	190.5	212.7	31.8
OPA830IDBVT	SOT-23	DBV	5	250	190.5	212.7	31.8
OPA830IDR	SOIC	D	8	2500	346.0	346.0	29.0

DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



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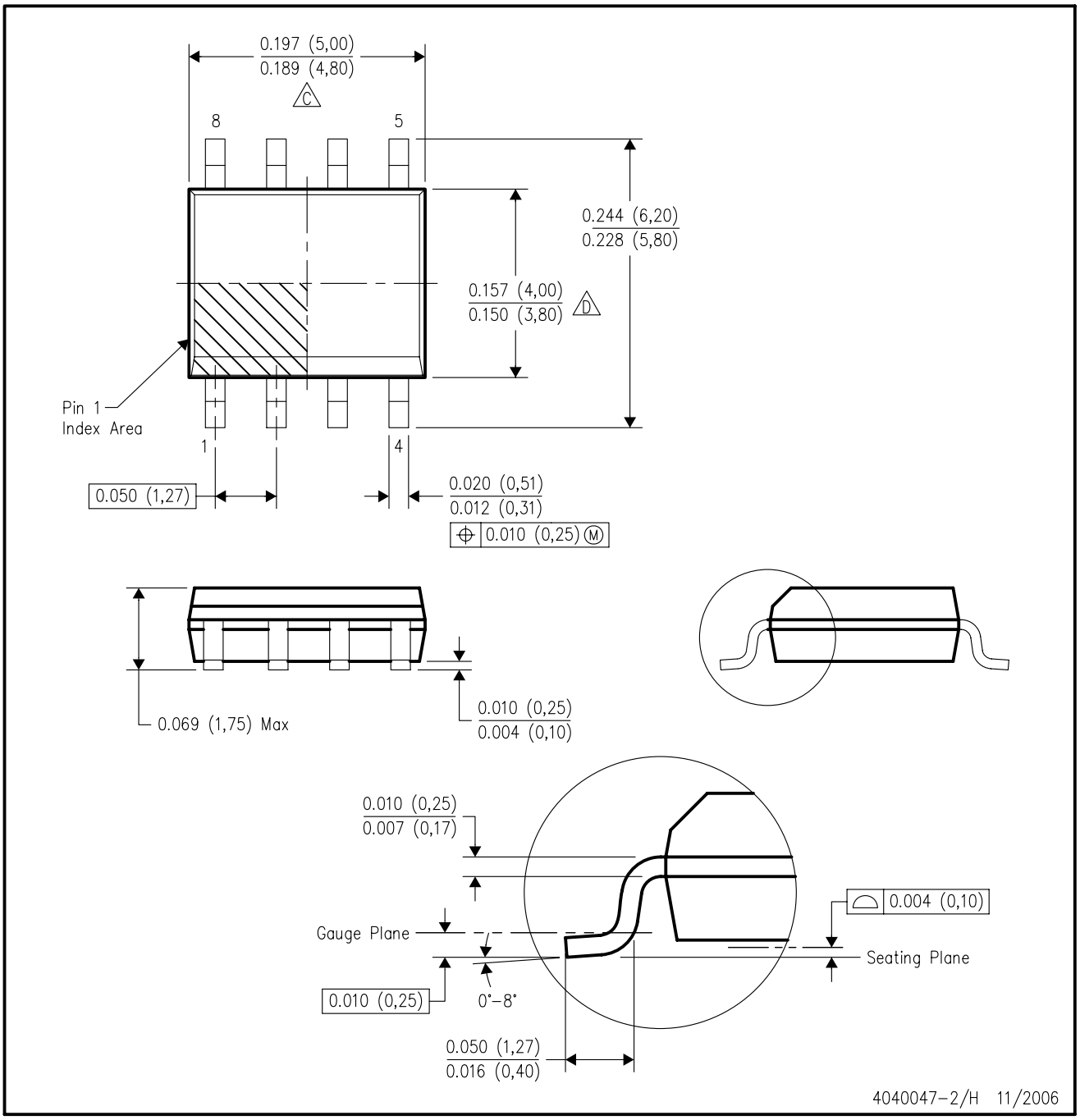
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

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